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Cache and Memory Design Considerations for the Intel486™ DX2 Microprocessor

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Cache and Memory Design Considerations for the Intel486™ DX2 Microprocessor

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1.0 INTRODUCTION

This section discusses CPU performance optimization techniques for the Intel486™ DX2 microprocessor. The reader should be familiar with the Intel486™ DX microprocessor as well as knowledgeable about memory systems and cache architectures. For further reference, the reader is directed to the following documents and application notes (corresponding Intel order number is shown in parentheses):

- Intel486™ DX2 Microprocessor Data Book (241245-001)
- Intel486™ DX Microprocessor Data Book (240440-004)
- Intel486™ DX Microprocessor Hardware Reference Manual (240552-001)
- Cache Tutorial 1991 (296543-002)
- AP447: A Memory Subsystem for the Intel486™ Family of Microprocessors including Second Level Cache (240799-002)
- 485TurboCache Module Intel486™ DX Microprocessor Cache Upgrade (240722-002)

2.0 The High-Performance Intel486™ DX2 Microprocessor

The Intel486 DX2 Microprocessor is functionally equivalent to the now-familiar Intel486™ DX Microprocessor. However, the Intel486 DX2 CPU's internal core runs at twice the frequency of its external bus. This architecture enables a very high level of performance while, at the same time, maintaining straightforward system design.

The Intel486 DX2 CPU is partitioned such that the cache and write buffers operate at the full core speed as illustrated in Figure 2.1. As such, the processor is only slowed to the external bus speed on cache misses and when the write-buffers are full. The Intel486 DX2 CPU's external bus interface is identical to its predecessor, i.e. all system cycles emanating from the CPU look exactly as if they would from the Intel486 DX CPU. The Intel486 DX2 microprocessor includes additional features such as JTAG boundary scan and power-down capability that are not covered in this section.

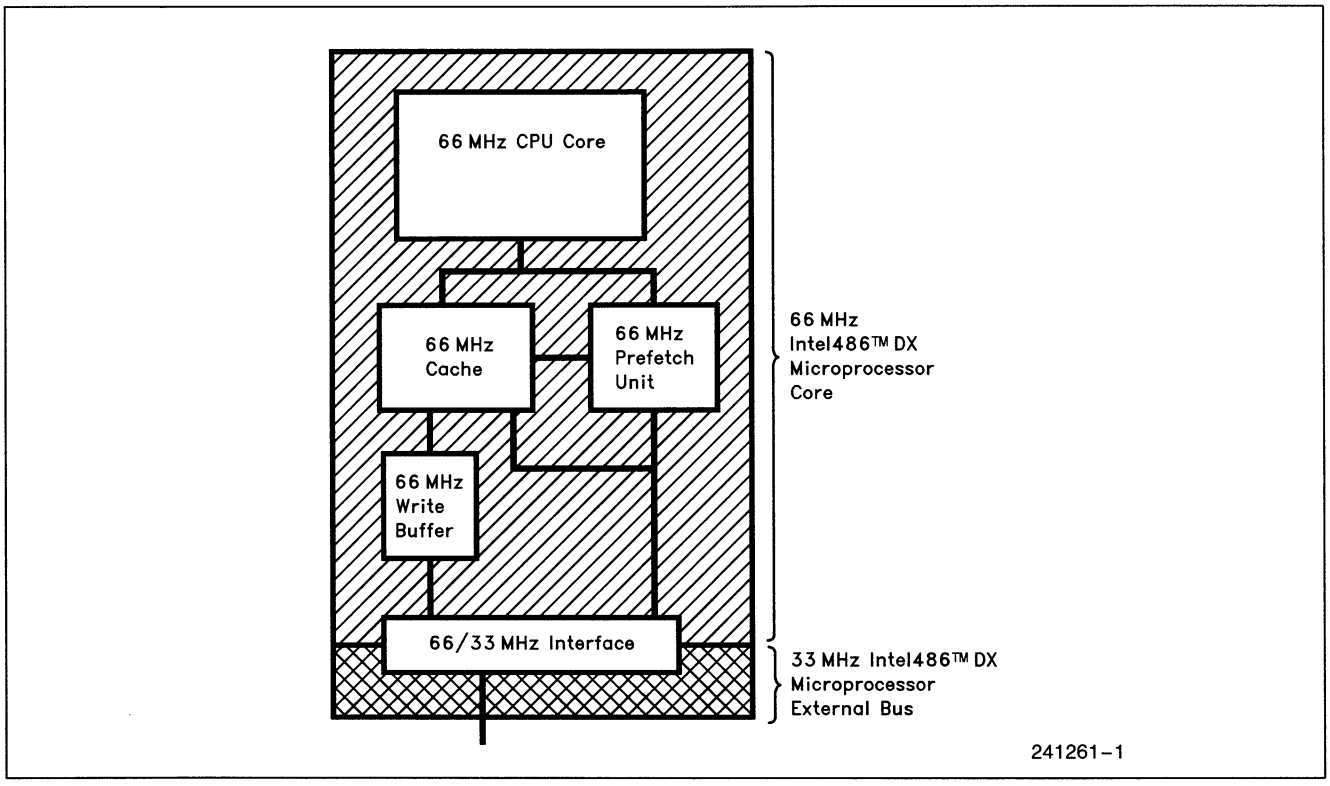

Figure 2.1. The 66MHz Intel486™ DX2 CPU Internal Architecture

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UNIX is a trademark of UNIX System Laboratories.
Lotus, 123 are trademarks of Lotus Development Corporation.
Turbo C is a trademark of Borland International.
AutoCAD is a trademark of AutoDesk, Inc.

Performance optimization for the Intel486 DX2 CPU is subtly different than for the Intel486 DX CPU due to the difference in the internal architecture. This is evident if you consider that external memory latencies now affect the full speed core by twice as many CPU clocks (refer to Figure 2.2). In other words, the memory system should really be designed to satisfy the data throughput demands of a 50/66MHz CPU. The next few sections examine the situation in detail so that educated trade-offs can be made during system design. The discussions will focus on CPU-cache memory performance; I/O performance and other architectural issues are not addressed in this applications note.

In an ideal system, all CPU cycles operate at zero-wait states and the theoretical maximum performance of the CPU is achieved. However, short of spending a lot of money on SRAMs, a real system always falls short of the ideal zero wait-states. There are many cache-memory designs that differ in both architecture and implementation. However, it may be impossible to design a system that performs better than all others across all applications; different applications generate different types of CPU bus activity and the cache-memory system will perform differently in each case. A range of statistical parameters may be used to illustrate this point:

- Internal Cache (L1) Hit Rate
- Number of prefetches
- Number of operand reads
- Number of operand writes
- Bus Utilization (amount of time spent using the CPU bus).

These parameters are examined next and will be useful information for cache-memory design trade-offs.

2.1 Internal Cache Hit Rates

The Intel486 DX2 CPU maintains the same unified code/data, four-way interleaved, 8K-byte internal cache as the Intel486 DX CPU. The internal cache (L1) hit rate is shown in Figure 2.3 for some different operating systems and applications. These hit rates were obtained from instruction traces captured from specific applications. Note that the L1 hit rate for the Intel486 DX2 CPU will be almost identical to that for the Intel486 DX CPU; the 2X-internal frequency does not significantly alter the cache miss statistics.

The DOS applications included Auto Cad, Lotus123, Excel, Turbo C, and Flight Simulator. Lotus123 had the highest hit rate at 99% while Auto Cad was the lowest at 89.6%. The Windows 3.0 results included instructions executed while clipping an image, drawing a dialog box, executing Excel and while executing Pagemaker. The category UNIX-iSPEC refers to applications within the UNIX SPEC benchmark suite that are mostly integer intensive, whereas UNIX-fSPEC refers to those which are floating point intensive. The last category UNIX-TP1 refers to the hit rates typical while running the TP1 transaction processing benchmark.

These results illustrate the different nature of different software on the bus characteristics. Single-threaded DOS applications have a typically higher hit rate compared to the multi-tasking nature of UNIX and Windows benchmarks. The UNIX floating point benchmarks show the lowest hit rates; this is partly due to the large data structures typical of floating point applications that do not fit well into the L1 cache. It is also due to the nature of the operations performed on those data structures; i.e. the application does not exhibit very much temporal or spatial locality.

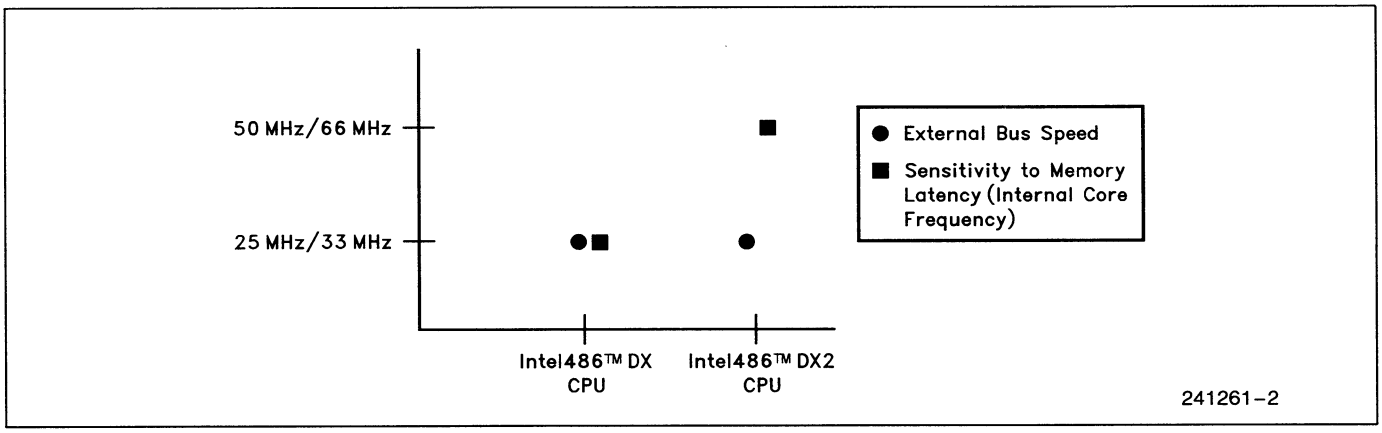


Figure 2.2. The Intel486™ DX2 Microprocessor is More Sensitive to Memory Latency than Its Predecessor

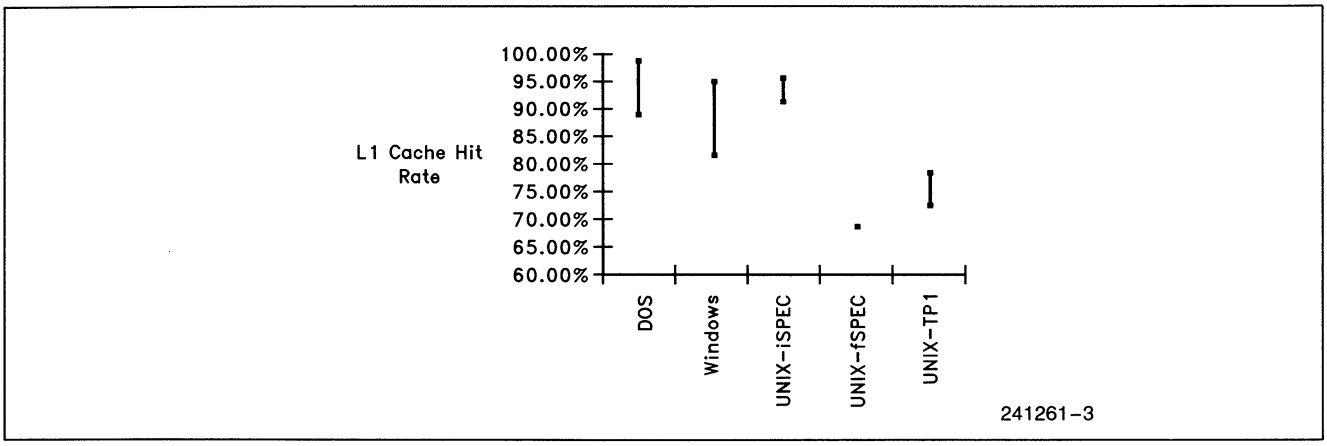


Figure 2.3. There will be a Range of L1 Hit Rates for Different Applications/Operating Systems

TP1 is a UNIX multiuser multithreaded application with heavy amounts of disk and I/O as well as computation. The L1 cache hit rate is low since it has many active contexts due to multiple requests per user.

High L1 hit rates are typical of many prevalent and commonly used DOS benchmarks - some have hit rates approaching 100%. This is unfortunate since they fail to properly account for the more realistic external cache and memory demands of most DOS and Windows applications. These demands will continue to be true with the advent of newer graphical-user-interface-based multi-tasking operating systems and applications. With these benchmarks, there is a danger of misrepresenting system performance for the Intel486 DX microprocessor. For the Intel486 DX2 microprocessor, this misrepresentation can be even more damaging since L1 cache misses incur a penalty that is twice the number of external clock cycles - since the CPU core now runs twice as fast internally. In other words, the Intel486 DX2 CPU is twice as sensitive to wait states compared to the Intel486 DX CPU. To properly gauge the external cache and memory performance, more demanding benchmarks (e.g. UNIX SPECmarks) or real application benchmarks should be used.

2.2 Bus Cycle Mix

Different applications cause the CPU to generate a different number of reads, writes and instruction prefetches. The reads and prefetches are filtered by the internal L1 cache before reaching the external CPU bus. All writes propagate through to the external bus since the internal cache follows a write-through protocol. This is shown in Figure 2.4 for an instruction trace captured from an integer SPEC benchmark.

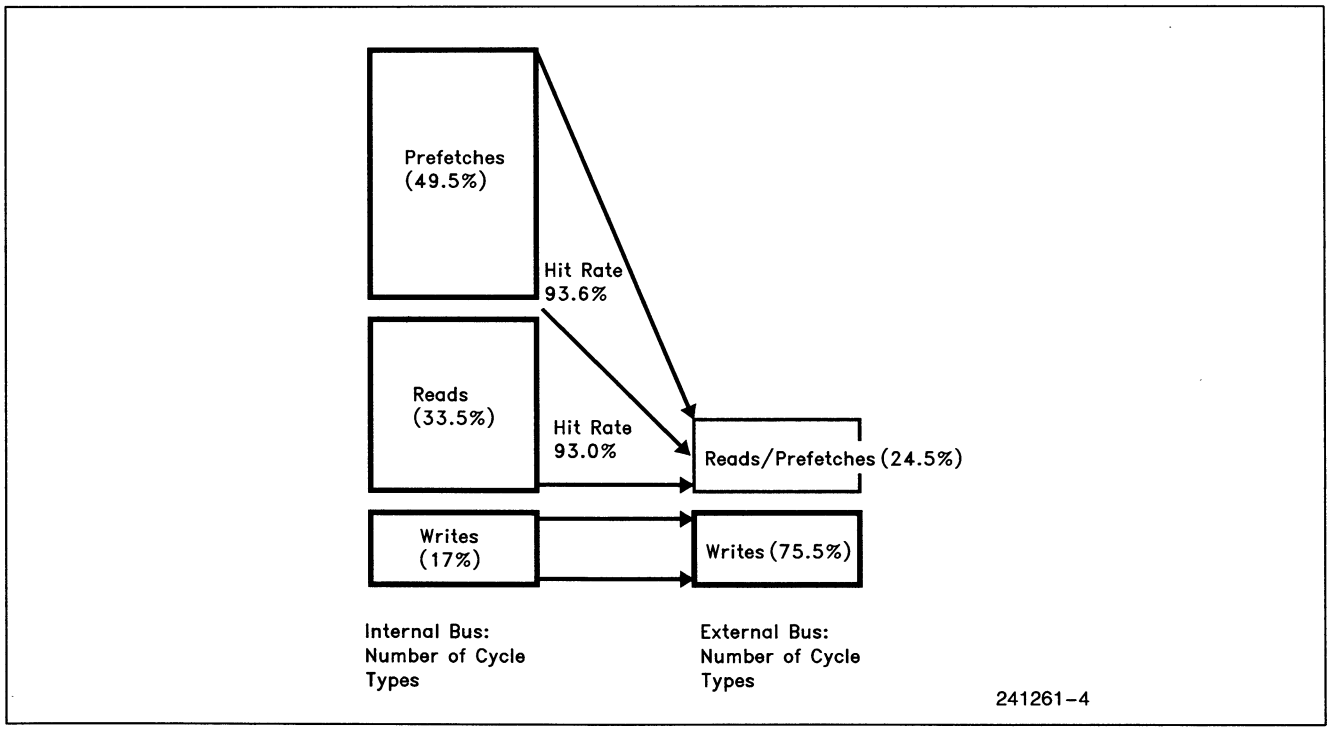


Figure 2.4. The Effect of L1 Cache Hits on the External Bus Cycle Mix for an Integer SPEC Benchmark

As with the Intel486 DX CPU, the bus cycle mix for the Intel486 DX2 CPU consists of mostly write cycles. However, the exact ratio of reads to writes is again application dependent. For example, for Lotus123 that has a L1 hit rate of 99%, writes make up 99.5% of external bus cycles.

2.3 Bus Utilization

Bus utilization refers to the amount of time that the CPU spends executing bus cycles for a given application. It is a measure of the amount of bus traffic generated by a particular application on the CPU's external bus. This metric is illustrated in Figure 2.5 where the CPU bus is busy for 75% of the twelve external clock cycles shown.

Bus utilization is dependent on the application and the external cache/memory system. Different applications generate different amounts of bus traffic. For example, some applications may have small data structures that fit easily within the internal cache and therefore smaller amounts of external bus cycles are generated.

The Intel486 DX2 CPU will have a larger percentage of bus utilization for the same application as compared to the Intel486 DX CPU. This is due to the faster CPU core that can now operate twice as fast and that will try to generate twice as many bus cycles in the same amount of time. However, since the external CPU bus remains at a 1X-frequency, it experiences heavy amounts of bus traffic as it trys to keep up with the 2X-internal core. In other words, with faster internal core execution, less time is spent idling on the external bus.

Different external cache/memory systems also affect the bus utilization; faster cache/memory systems allow CPU cycles to complete faster and therefore free up the bus more.

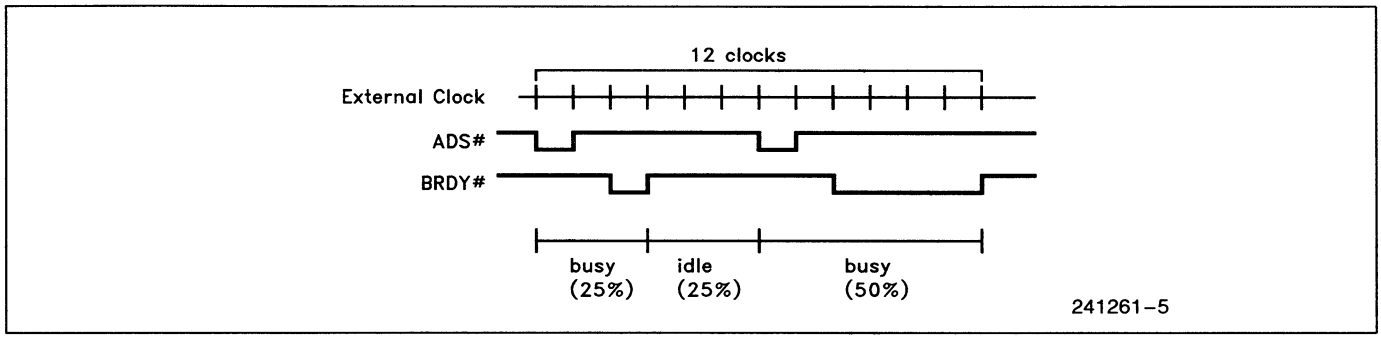


Figure 2.5. Definition of Bus Utilization

2.4 Profiles of Some Applications

The Intel486 DX2 CPU bus characteristics of some different applications and operating systems are shown in Tables 2.1 through 2.3. These results are derived from traces captured from the actual applications. These traces were subsequently used in a CPU-cache-memory simulator to extract the desired information. The results shown here assume an ideal zero wait-state memory system; i.e. all bus cycles complete in zero wait-states.

Table 2.1. Bus Profiles of UNIX Applications with a Zero Wait-State Memory System

UNIX Applications	SPEC1	GCC	UNIXMIX1
Total Number of CPU clocks simulated	12.14M	12.54M	12.44M
Overall L1 hit rate	91.4%	90.5%	94.3%
Prefetch hit rate	93.6%	91.7%	94.8
Read hit rate	93.0%	90.3%	94.2%
Write hit rate	82.0%	85.7%	93.5%
Number of external bus cycles	1.12M	0.882M	1.18M
% bus code prefetches	14.5%	22.6%	10.2%
% bus data reads	10.0%	20.0%	8%
% bus data writes	75.5%	57.4%	81.8%
Bus Utilization	51.6%	46.4%	51.4%

Table 2.2. Bus Profiles of Windows Applications with a Zero Wait-State Memory System

Windows Applications	Word	Excel—Calc	Pagemaker
Total Number of CPU clocks simulated	27.02M	7.39M	30.06M
Overall L1 hit rate	95.2%	78.4%	88.1%
Prefetch hit rate	96.9%	76.0%	81.8%
Read hit rate	98.0%	85.7%	95.2%
Write hit rate	87.7%	69.7%	83.5%
Number of external bus cycles	2.43M	0.654M	3.04M
% bus code prefetches	4.2%	27.9%	19.3%
% bus data reads	3.4%	15.1%	6.7%
% bus data writes	92.4%	57.0%	74%
Bus Utilization	40.9%	60.1%	56.0%

Table 2.3. Bus Profiles of DOS Applications with a Zero Wait-State Memory System

DOS Applications	Excel	Turbo C	Auto Cad
Total Number of CPU clocks simulated	11.1M	13.9M	16.1M
Overall L1 hit rate	98.2%	95.6%	89.3%
Prefetch hit rate	98.8%	94.2%	87.7%
Read hit rate	97.9%	98.1%	96.5%
Write hit rate	97.4%	93.8%	81.3%
Number of external bus cycles	1.06M	1.18M	1.77M
% bus code prefetches	2.1%	11.2%	11.8%
% bus data reads	3.1%	3.0%	4.0%
% bus data writes	94.8%	85.8%	84.2%
Bus Utilization	41.0%	40.6%	55.5%

The UNIX applications are described as:

- SPEC1: A mixture of integer SPEC benchmark suite programs running concurrently.
- GCC: SPEC benchmark suite GNU C compiler, compiling itself.
- UNIXMIX1: A mixture of UNIX utility programs like awk and grep, running concurrently.

The Microsoft Windows 3.0 applications are described as:

- Word: Microsoft Word for Windows converting a document for import (no VGA activity, includes kernel calls).
- Excel—Calc: Microsoft Excel for Windows running a calculation.
- Pagemaker: Pagemaker for Windows formatting a document (no VGA activity, includes kernel calls)

The three DOS applications shown are described as:

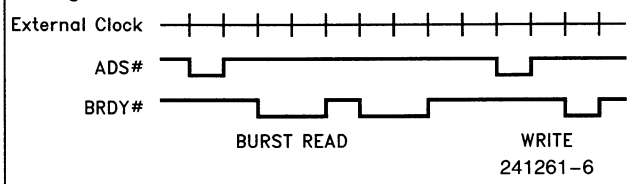
- Excel: Microsoft Excel (DOS version) recalculating a spreadsheet.
- Turbo C: Borland's Turbo C compiler compiling a large C program.
- Auto Cad: Auto Desk's Auto Cad program computing and displaying a drawing (reason for low hit rate)

Note that most DOS applications will typically use the external bus much less than UNIX or Windows applications. On the other hand, heavy duty DOS applications such as Auto Cad will actually exhibit a larger demand for the external bus similar to the demands of UNIX and Windows. Also, recall that the bus utilization numbers shown assume a zero wait-state memory system; more realistic external cache/memory systems with a finite number of wait-states will actually experience a larger percentage of bus utilization. Finally, note that since the L1 hit rate for the DOS applications is high, the external bus mix consists of mostly writes.

2.5 Wait States Explained

Now that we have considered the characteristics of L1 hit rates, bus cycle mix and utilization, we can examine the impact that the cache-memory system has on overall Intel486 DX2 CPU performance. To examine these effects, traces were captured from three applications (one from each operating environment) and were used in a CPU-cache-memory simulator to measure the CPU performance under different conditions. The traces used were SPEC1 (UNIX), Pagemaker (Windows) and Turbo C (DOS). The simulator used is an accurate and convenient method of comparing performance by varying different parameters independently. This allows us to develop some heuristic rules to guide system design. Before continuing, the following convention is defined to denote memory performance:

Notation Convention:
A memory system's performance is abbreviated as:
Lead-off clocks - Burst 2 - Burst 3 - Burst 4, Write clocks
e.g. 3-1-2-1, 3 would look like:



A zero-wait-state case corresponds to a 2-1-1-1, 2 memory system.

Figure 2.6. Memory Performance Notation

2.5.1 THE IDEAL ZERO WAIT STATE MEMORY SYSTEM

As a starting point, the ideal zero-wait-state memory system was characterized for three applications. For I/O cycles, it was assumed that a constant 8 wait-states were required. Since the I/O instructions were a small portion of the instruction traces used, any inaccuracy due to this assumption will be insignificant.

The total execution times reported are as follows:

Table 2.4. Number of Internal Clocks (millions) Needed to Complete Application Trace

	SPEC1	Pagemaker	Turbo C
Intel486 DX CPU	10.76	26.68	13.34
Intel486 DX2 CPU	12.14	30.06	13.90

As an example, we can now compare the actual time required to complete the applications between a 66MHz Intel486 DX2 CPU and a 33MHz Intel486 DX CPU. The number of clock cycles is multiplied by 15ns for the Intel486 DX2 CPU and by 30ns for the Intel486 DX CPU.

Table 2.5 Total Execution Time in Seconds

	SPEC1	Pagemaker	Turbo C
Intel486 DX CPU	323 ms	800 ms	400 ms
Intel486 DX2 CPU	182 ms	451 ms	209 ms
Performance Increase	+77%	+77%	+91.4%

Note that although the Intel486 DX2 CPU's internal clock rate is twice that of the corresponding Intel486 DX CPU, the relative improvement is less than 100%. This is due to cache miss reads and write cycles that run at the external bus speed. Note that the improvement is much greater for Turbo C which has a lower cache miss rate and low bus utilization.

2.5.2 ADDING WAIT STATES

As wait states are added to the ideal zero wait state memory system, performance degrades. Three memory parameters are of interest in characterizing the memory performance. They are:

- Number of wait states added to the first ready of a read (a.k.a. the lead-off cycle). e.g. One wait-state with zero wait-state burst = 3-1-1-1
- Number of wait states during the remainder of the burst cycle. e.g. a zero wait-state lead-off with a one wait-state burst = 2-2-2-2
- Number of wait states on a write cycle. e.g. a one wait-state write takes three clocks.

To examine the impact of adding wait-states to each of the parameters above, three series of simulations are done where wait states are added to each memory parameter separately while the other memory parameters are held constant:

	Zero wait-states	1 wait-state	2 wait-states	3 wait-states
• Lead-off Series:	2-1-1-1, 2	3-1-1-1, 2	4-1-1-1, 2	5-1-1-1, 2 . . .
• Burst Series:	2-1-1-1, 2	2-2-2-2, 2	2-3-3-3, 2	2-4-4-4, 2
• Write Series:	2-1-1-1, 2	2-1-1-1, 3	2-1-1-1, 4	2-1-1-1, 5 . . .

As the number of wait states increases, the number of clocks needed to complete the application increases (and the CPU performance decreases). This series of measurements is used to separate out the dependency of the CPU performance on the different memory parameters. This information is useful for subsequent external cache/memory design trade-offs.

The number of clocks needed to complete the application relative to the zero wait-state case is referred to as the relative total execution time. This metric will be used in the following graphs instead of the reciprocal of total execution time which would be CPU performance; this is so that any inherent linear relationships between wait-states and execution time can be more easily recognized. To translate the total execution time back to CPU performance, the following table is provided for convenience (100% refers to the zero wait-state case):

Table 2.6. CPU Performance versus Total Execution Time

Total Execution Time	100.00%	110.00%	120.00%	130.00%	140.00%	150.00%	160.00%
CPU Performance	100.00%	90.91%	83.33%	76.92%	71.43%	66.67%	62.50%

Figures 2.7 and 2.8 show the total execution time as wait states are added for the SPEC1 trace described earlier.

As would be expected, as wait states are added, the relative total execution time for the Intel486 DX2 CPU increases faster than the Intel486 DX CPU. (however, note that the absolute total execution time for a Intel486 DX2 CPU will never be greater than a Intel486 DX CPU of the same external bus speed). Also note that the order of importance of the memory parameters changes between the Intel486 DX and the Intel486 DX2 CPU. For the Intel486 DX CPU, burst performance is the most important, with read-lead-off performance being slightly more important than writes. This conclusion was presented in Chapter 4 of the original Intel486 DX Microprocessor Hardware Reference Manual (Order Number 240552-001). However for the Intel486 DX2 CPU, while burst performance is still the most important, write performance becomes more important than read-lead-off performance.

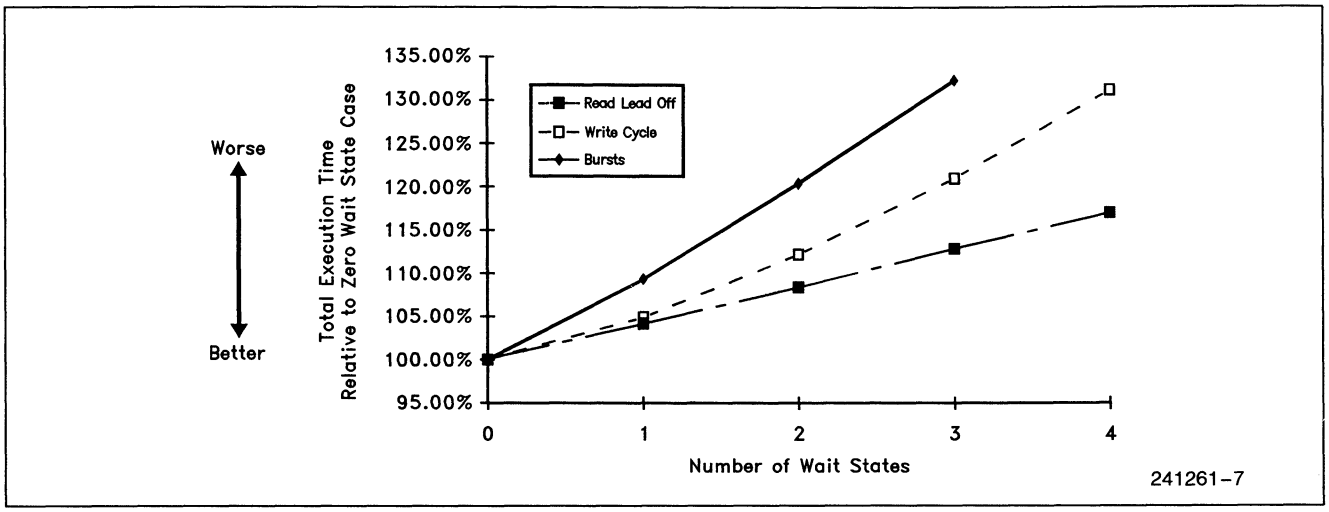


Figure 2.7. Intel486 DX2 CPU Performance Degradation as Wait States are Added - for the SPEC1 Application Trace (UNIX)

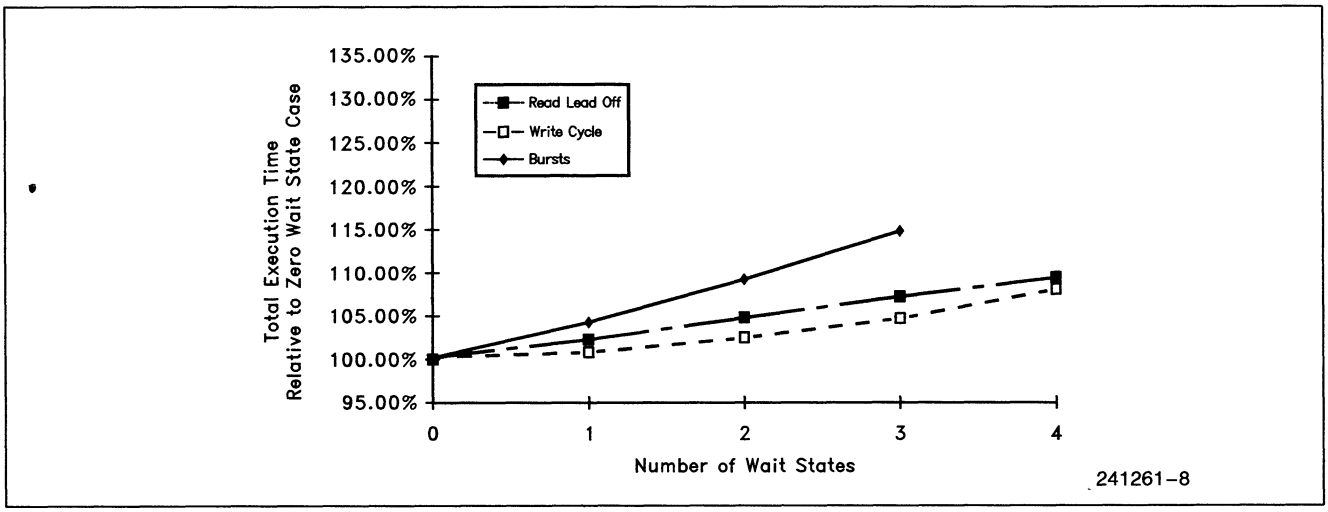


Figure 2.8. Intel486 DX CPU Performance Degradation as Wait States are Added - for the SPEC1 Application Trace (UNIX)

Figures 2.9 and 2.10 show the total execution time as wait states are added for the GCC trace described earlier.

Compared to the results for the SPEC1 application trace, the GCC results with the Intel486 DX2 CPU still show the burst cycles as being the most sensitive to wait states. However, note that the lead-off cycle is now more important than write cycles. This is due to the small percentage of bus writes (57.4%) while running the GCC application as compared with the SPEC1 trace.

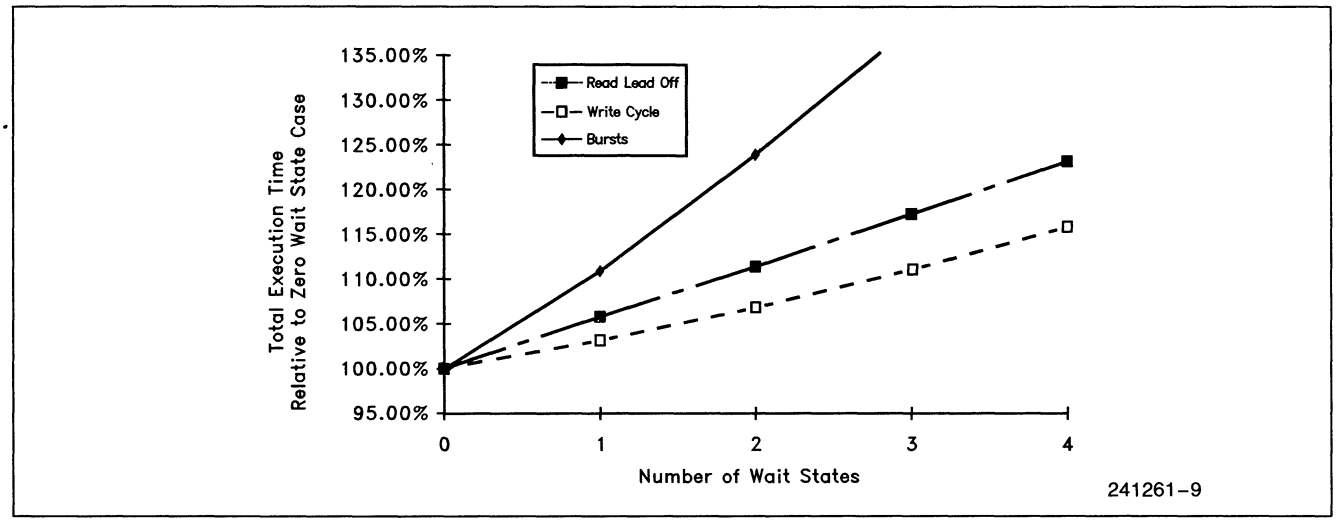


Figure 2.9. Intel486 DX2 CPU Performance Degradation as Wait States are Added - for the GCC Application Trace (UNIX)

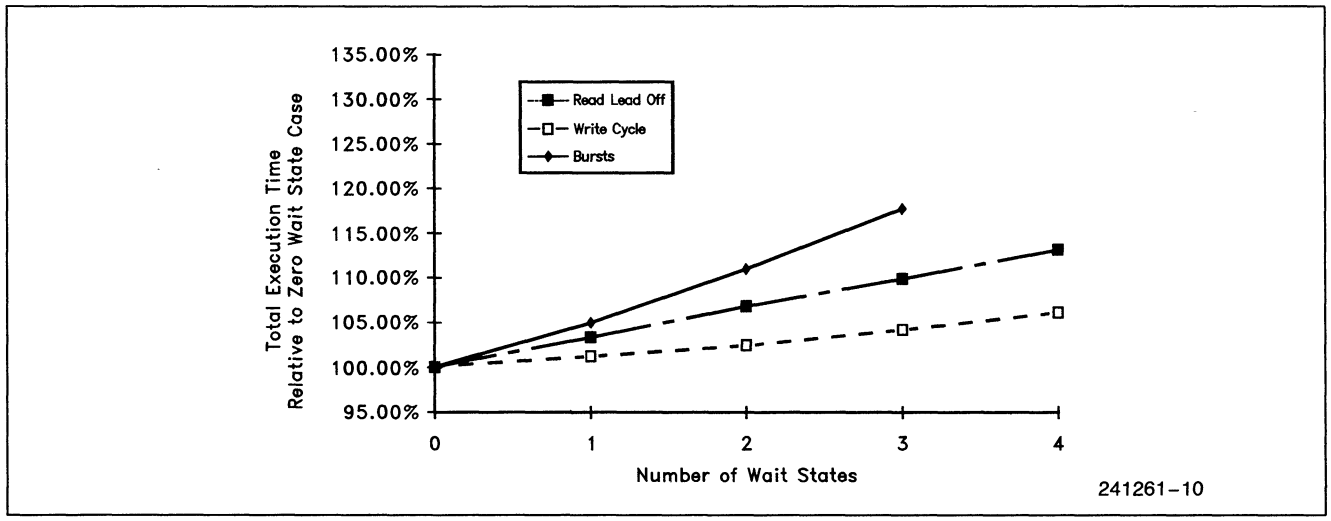


Figure 2.10. Intel486 DX CPU Performance Degradation as Wait States are Added - for the GCC Application Trace (UNIX)

The results for the Pagemaker Application under Windows are shown in Figures 2.11 and 2.12.

The same conclusions can be made for the Pagemaker application under Windows as for the SPEC1 results earlier. Basically, the degradation of the Intel486 DX2 CPU's relative execution time increases faster as wait-states are added as compared to the Intel486 DX CPU.

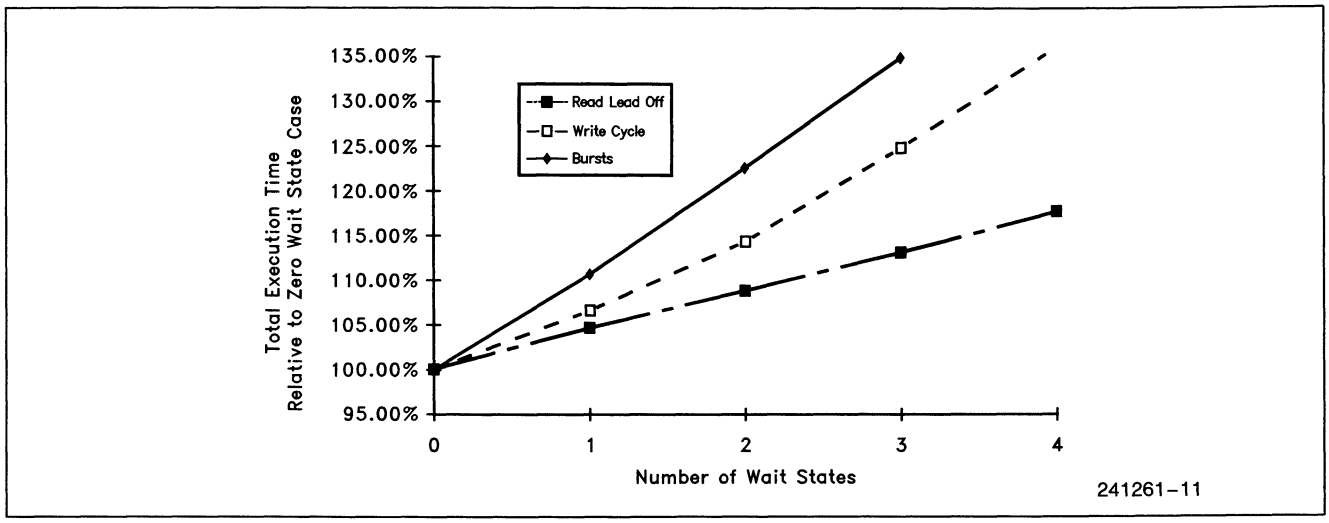


Figure 2.11. Intel486 DX2 CPU Performance Degradation as Wait States are Added - for the Pagemaker Application Trace (Windows)

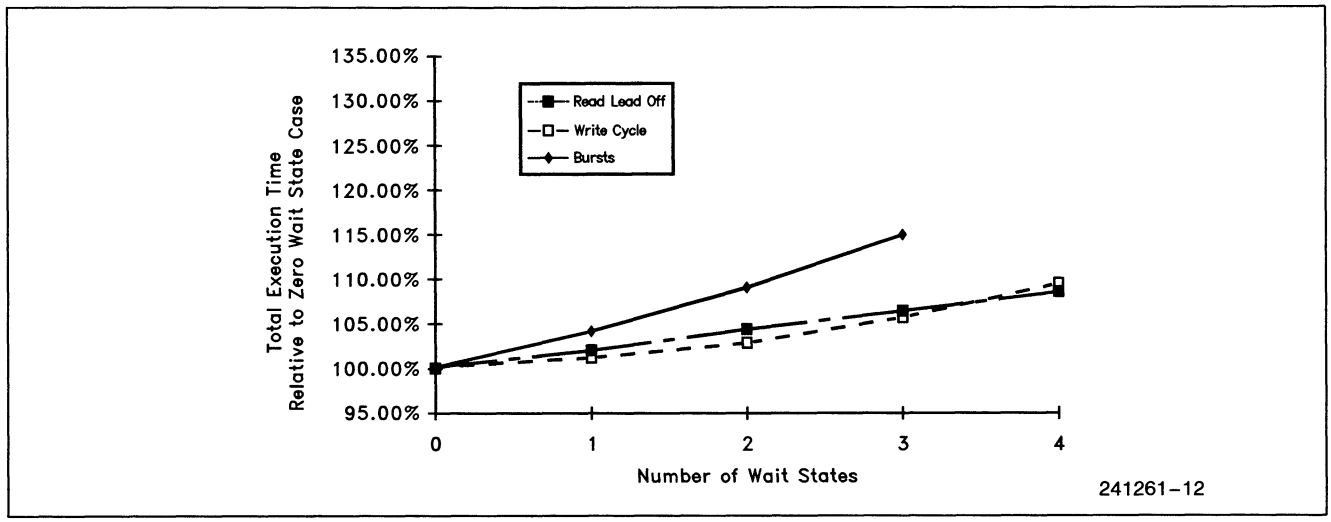


Figure 2.12. Intel486 DX CPU Performance Degradation as Wait States are Added - for the Pagemaker Application Trace (Windows)

Finally, the results for the Turbo C application under DOS are shown in Figures 2.13 and 2.14.

The rate of performance degradation for the Intel486 DX2 CPU with the Turbo C application is less than the UNIX and Windows examples. This is due to the lower external bus utilization of the application. However, the degradation is still about twice what it is for the Intel486 DX CPU. Note that the write importance is about equal to the burst importance in this case. This can be attributed to the greater percentage of writes in the bus cycle mix for this application.

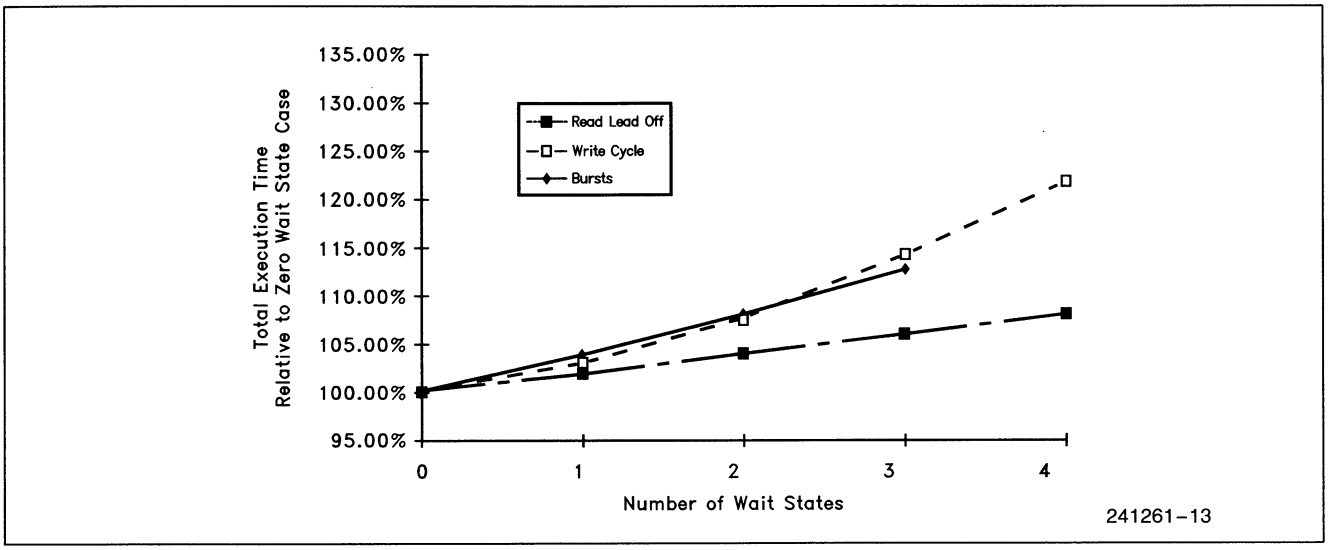


Figure 2.13. Intel486 DX2 CPU Performance Degradation as Wait States are Added - for the Turbo C Application Trace (DOS)

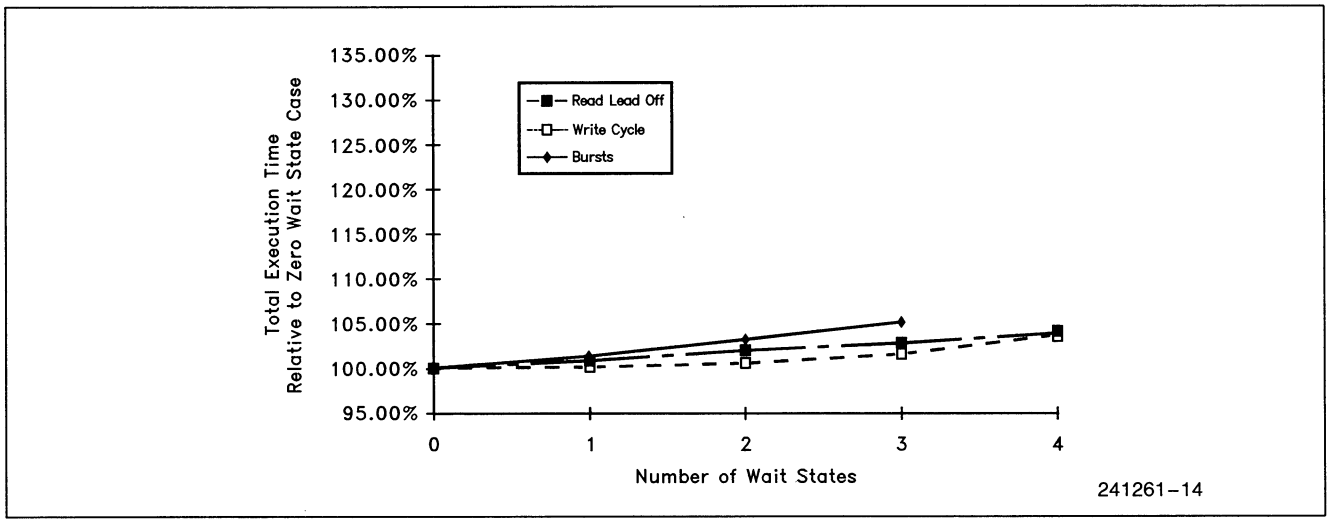


Figure 2.14. Intel486 DX CPU Performance Degradation as Wait States are Added - for the Turbo C Application Trace (DOS)

2.5.3 WAIT STATES AND CPU STALLS

The main reason why the relative performance of the Intel486 DX2 CPU degrades faster than the Intel486 DX CPU is that for every external wait state, two internal clock delays are caused. In fact, a zero wait state cycle on the external bus of the Intel486 DX2 CPU is already a two-wait state cycle as experienced by the 2X-clock internal core as shown in Fig. 2.15. The imaginary 2X-clock versions of the signals ADS# and BRDY# illustrate what the cycle might have looked like if the internal bus frequen cy was equal to the external.

Extending this fact, this means that a one wait-state cycle for the Intel486 DX2 CPU is actually equivalent to a four wait-state cycle for the 2X-clock internal CPU core.

The internal cycle start indication conditions may also have a one internal clock cycle synchronization penalty if it is active in the wrong phase of the external clock (also shown in Figure 2.15).

As the effective number of wait states increases, the CPU will stall program execution differently for each of the three memory parameters described above. The stall conditions for each memory parameter are elaborated below.

2.5.3.1 Delay Till First Ready of a Read

Wait states incurred on the first ready of a external read (the lead-off cycle) affect both data reads and code prefetches. For data reads, the CPU's execution is stalled under most conditions; no other operation can happen in parallel until the first ready of the line fill is received. For code prefetches, execution is stalled if the processor is fetching code as a result of a code branch (therefore flushing the prefetch buffers).

For most applications, the read lead-off delay increases the execution time the least compared to the other parameters. This is because writes cycles usually make up the dominant share of the bus cycles. However, there are exceptions to this case; for example, with the GCC trace, only 57.4% of the bus cycles were writes.

2.5.3.2 Wait states on Bursts

Adding wait states to the burst cycle increases the execution time the most. The burst is usually the result of a cache line fill or a code prefetch. Adding wait states to this parameter ties up the bus for the longest periods of time compared to adding the same number of wait states to the other parameters. As a result, all subsequent external bus requests are stalled as the CPU waits for the burst cycle to complete. These include stalls while the CPU waits to do a read cycle. A longer burst cycle also delays the rate at which the internal write buffers can be emptied since the write buffers must also wait for the external bus to free up. This causes stalls as described below for write cycles.

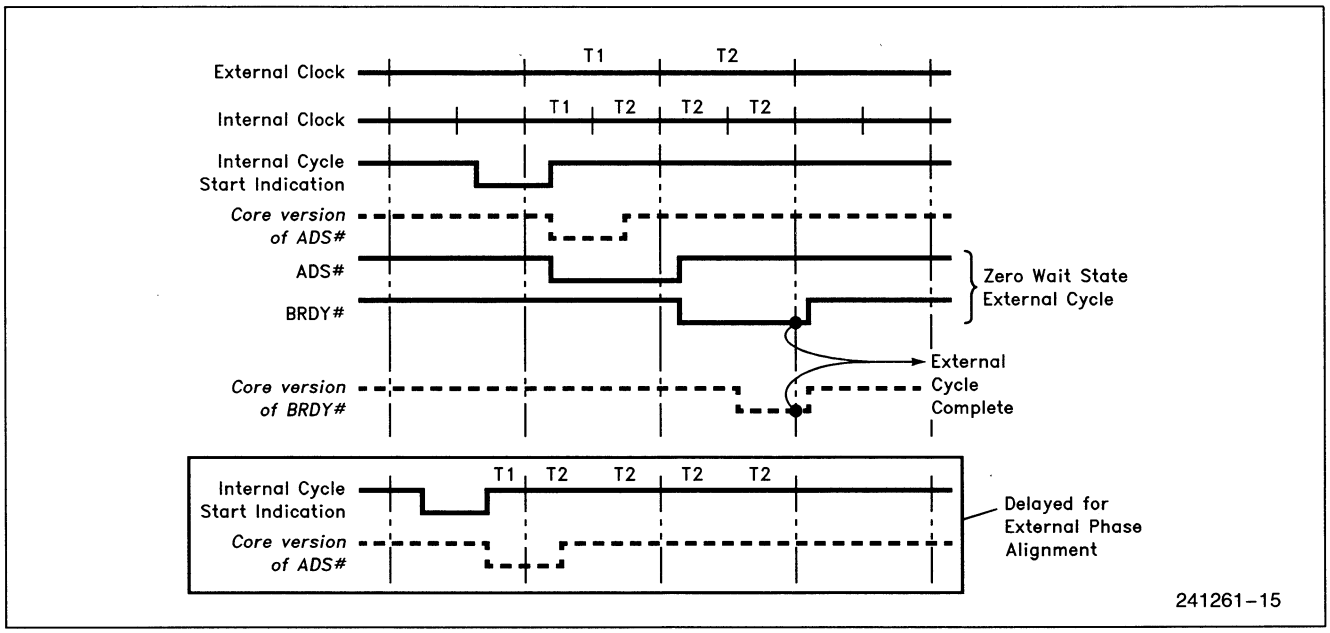


Figure 2.15. A Zero-Wait State Write for the Intel486™ DX2 CPU

Finally, longer code prefetch bursts will slow down CPU execution if the prefetch was a result of the prefetch queue being flushed. This is especially so if the instruction required extends beyond the first dword of the burst and therefore the CPU must wait for subsequent dwords before execution can start.

2.5.3.3 Write Wait States

There are three conditions under which a longer write cycle will stall CPU execution as additional wait states are added. These conditions are:

1. The write buffers are full and cannot accept any more writes.
2. A read cannot bypass the write buffers and must wait for them to be flushed.
3. A read bypasses the write buffers but must wait for an existing write cycle to complete.

Before these effects are elaborated, it is worthwhile to reexamine the operation of the internal write buffers.

The Intel486 DX2 CPU uses the same four-deep write buffers as the Intel486 DX CPU. The write buffers can accept data writes from the execution core as fast as one per clock. Once a write request is buffered, the internal unit that generated the request is free to continue processing. When all write buffers are full, any subsequent write transfer will stall inside the processor until a write buffer becomes available.

The bus interface unit can re-order pending reads in front of buffered writes. This is done because pending reads can prevent an internal unit from continuing, whereas buffered writes need not have a detrimental effect on processing speed. Writes are propagated to the external bus in the same first-in-first-out order in which they are received from the internal unit. However, a subsequently generated read request (data or instruction) may be reordered in front of buffered writes. As a protection against reading invalid data (reading stale data from a location in main memory when the location has been modified in the write buffers), this reordering of reads will only occur if all buffered writes are internal cache hits. Because an external read will only be generated for a cache miss, and will only be reordered in from of buffered writes if all such writes are internal cache hits, any read generated on the external bus will never read a location that is about to be written by a buffered write.

This reordering can only happen once for a given set of buffered writes, because the data returned by the read cycle could otherwise replace data about to be written from the write buffers.

The first condition that causes CPU stalls is when the write buffer is full. Write wait states decrease the rate at which the write buffer can be emptied. Since the Intel486 DX2 runs at a 2X-internal frequency, the likelihood of filling up the write buffers increases when compared to the Intel486 DX CPU as shown in Figure 2.16.

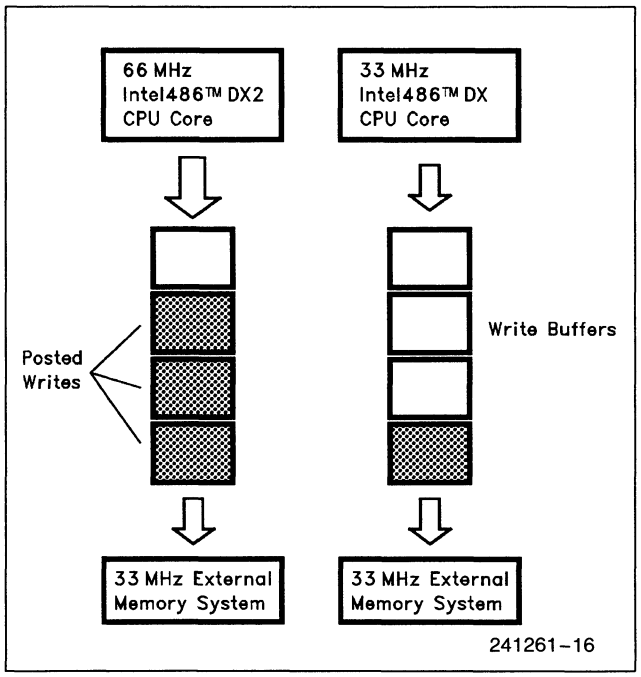


Figure 2.16. The Intel486 DX2 CPU's Write Buffers are More Heavily Used than the Intel486 DX CPU's

The second situation that degrades performance is during reads which cannot bypass the write buffers - either because the buffered writes were cache misses or because a read reordering had already occurred. These reads will be stalled until the write buffers are emptied. The more wait states required for writes on the external bus, the longer these stalls will last.

Finally, reads which can bypass the write buffers may be stalled by a write already in progress on the external bus. This condition is illustrated in Fig 2.17 for both the Intel486 DX and Intel486 DX2 CPUs. Note that for this example, although both the Intel486 DX2 and Intel486 DX CPUs take the same amount of time to complete the instruction stream, the Intel486 DX2 CPU is stalled longer (waiting for the write to complete) relative to its own internal 2X clock.

Out of the three conditions described above, stalls on write buffers full and stalls because of reads on busy writes dominate the increase in execution time as wait states are added to write cycles as shown in Table 2.7 for the SPEC1 trace. (The results shown in Figure 2.7 assume that the read and burst cycles complete in zero wait-states). These effects will be discussed again later when the addition of external write buffers is considered.

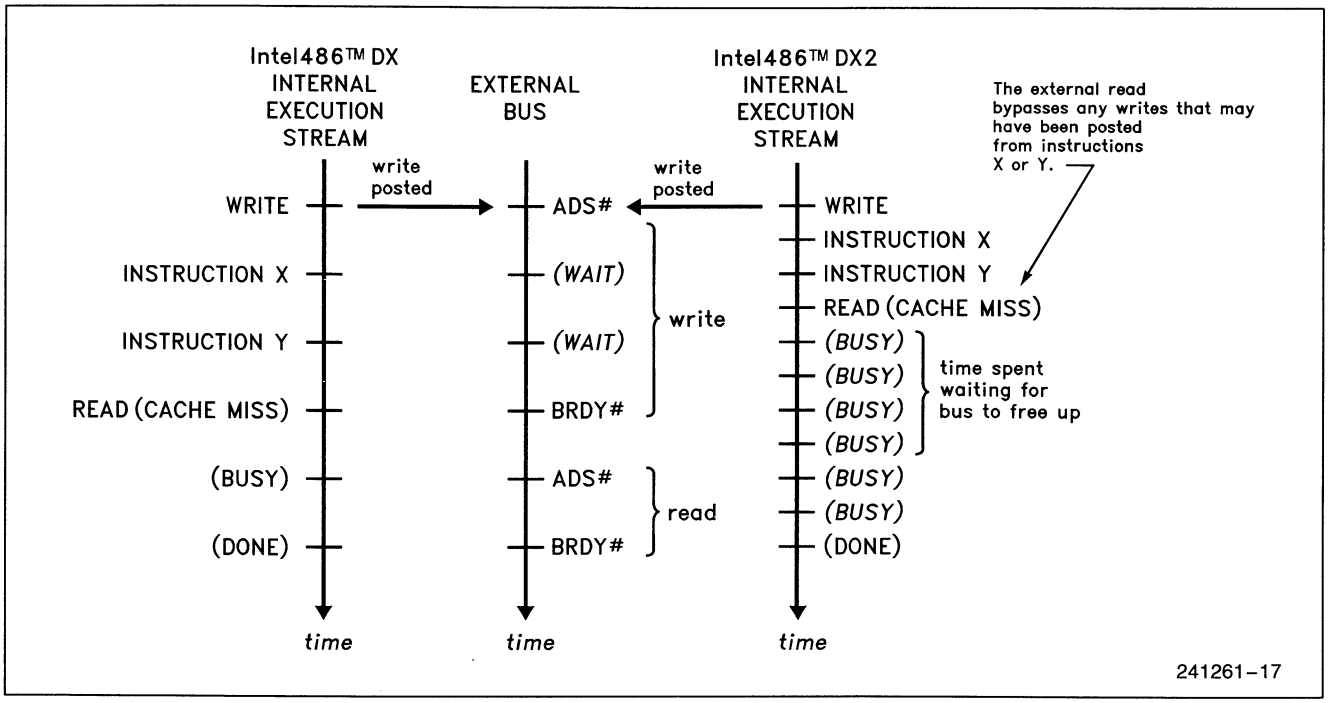


Figure 2.17. Reads Stalled as a Result of a Write Already In Progress

Table 2.7 Percentage of Total Execution Time Stalled under the Three Different Write Stall Conditions

	Intel486 DX CPU			Intel486 DX2 CPU		
Write wait states	**0**	**1**	**2**	**0**	**1**	**2**
Stalls on write buffers full	0.0%	0.1%	0.6%	1.0%	3.1%	6.5%
Reads cannot overtake writes	0.1%	0.1%	0.3%	0.3%	0.5%	0.5%
Stalls because of reads on busy writes	0.6%	1.3%	2.2%	2.4%	4.8%	7.5%

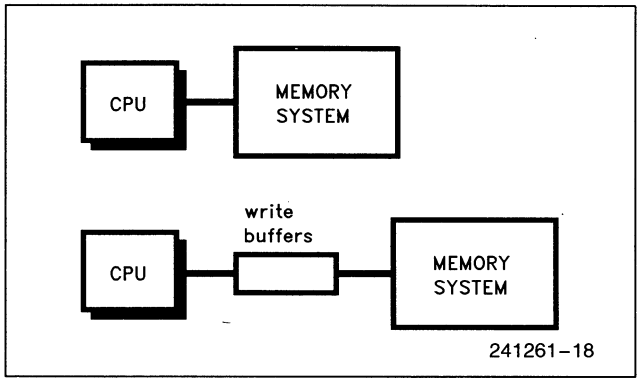


Figure 3.1 The Two Cacheless Intel486 DX2 CPU-Based Systems Considered

3.0 Memory Design Optimization

Some Intel486 DX2 CPU-based designs will include a memory system without an external cache. This section covers the design of such a cacheless memory system. Different memory architectures are discussed and the benefits of improving write performance through the addition of external write buffes will also be considered (see Figure 3.1).

Main memory performance will be important for external cache-based designs also, especially for applications with low external cache hit rates. It is recommended that the performance impacts of design choices in a cacheless memory design are understood even if you have already specified an external cache in your design.

As discussed in the previous sections, the Intel486 DX2 Microprocessor requires a fast memory system for optimum performance. Memory systems that may have been adequate for Intel486 DX CPU designs running DOS applications may be suboptimal for the Intel486 DX2 CPU, especially running today's more demanding operating systems and applications.

Main memory page-mode operation and interleaving techniques are important for Intel486 DX2 CPU performance. These are commonly used in existing, well-designed Intel486 DX CPU memory systems. However, some systems still use non-interleaved memory designs borrowed from Intel386 DX systems. These will be less than optimal for a high performance Intel486 DX2 CPU workstations design.

3.1 Page Mode DRAM

Page-mode main memory controllers can be implemented in several fashions. Typical memory systems utilize paging for all accesses - during the beginning of a read, during read bursts and during write cycles; i.e. the RAS# line is held active after all accesses and only returned inactive during a page miss. Alternatively, paging may be used only for the burst portion of a read cycle; the RAS# line always returns inactive after the read or write cycle has been completed. This method is more commonly used in conjunction with a write-back external cache as discussed in Section 4.4.

For read burst cycles, the 16-byte linefill of data or code will always lie within a DRAM page, thereby allowing the data or code to be strobed out of memory with a series of back-to-back CAS# pulses. Paging allows for a much faster burst cycle compared to the case where a full RAS#-CAS# cycle is required for each dword. A page mode burst read access to a single bank of memory is shown in Fig. 3.2.

A paged memory system also allows for faster back-to-back write cycles. As was true for the Intel486 DX CPU, the Intel486 DX2 CPU generates writes in strings of two, about 60%-70% of the time, and writes in strings of three about 40%-50% of the time. This bus characteristic accounts for a large page hit rate for writes; therefore, it is faster to perform the back-to-back write cycles in a fast page mode rather than performing a full RAS#-CAS# cycle for each write.

At this point, it is worthwhile to examine the page hit/miss ratio for the three applications considered in the previous section. These results are shown in Table 3.1 and assume no external cache and a page size of 8192 bytes.

Table 3.1 Page Hit Ratios

	SPEC1	Pagemaker	Turbo C
Read Page Hit	31.2%	26.4%	25.4%
Read Page Miss	68.8%	73.2%	74.6%
Write Page Hit	65.5%	68.8%	68.9%
Write Page Miss	34.5%	31.2%	31.1%

Note the low page hit ratio for CPU reads. This is due to the internal cache of the Intel486 DX2 CPU that filters read requests and tends to make the cache miss reads more randomly distributed throughout main memory.

3.2 Interleaving

Interleaving involves the use of more than one bank of memory; different banks are controlled separately. As an access is occurring, the other banks are being readied for the next access. Interleaving can be implemented in several ways. Horizontally interleaved banks generate accesses for consecutive locations in memory. For example, one bank can be designated as an odd dword and another for the even dword. Vertically interleaved banks separate large contiguous regions of memory between banks; i.e. multiple DRAM pages are open. Memory controllers often combine both methods.

Horizontal interleaving can be combined with paging to generate very quick burst reads. Two 32-bit banks can generate a zero wait-state burst as detailed in the Intel Applications Note AP447 "A Memory Subsystem for the Intel486™ DX Family of Microprocessors including Second Level Cache." Fig. 3.3 illustrates a burst read cycle from a paged-interleaved memory system. The signals CAS0# and CAS1# drive each of the two 32-bit banks of memory in this example.

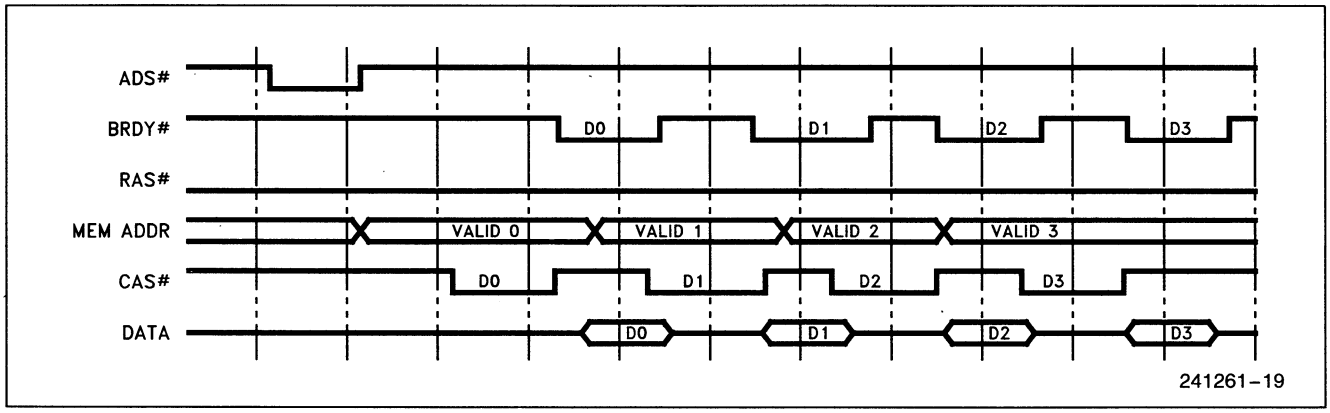


Figure 3.2. A Page Mode Burst Read (Page Hit on Lead-Off Cycle)

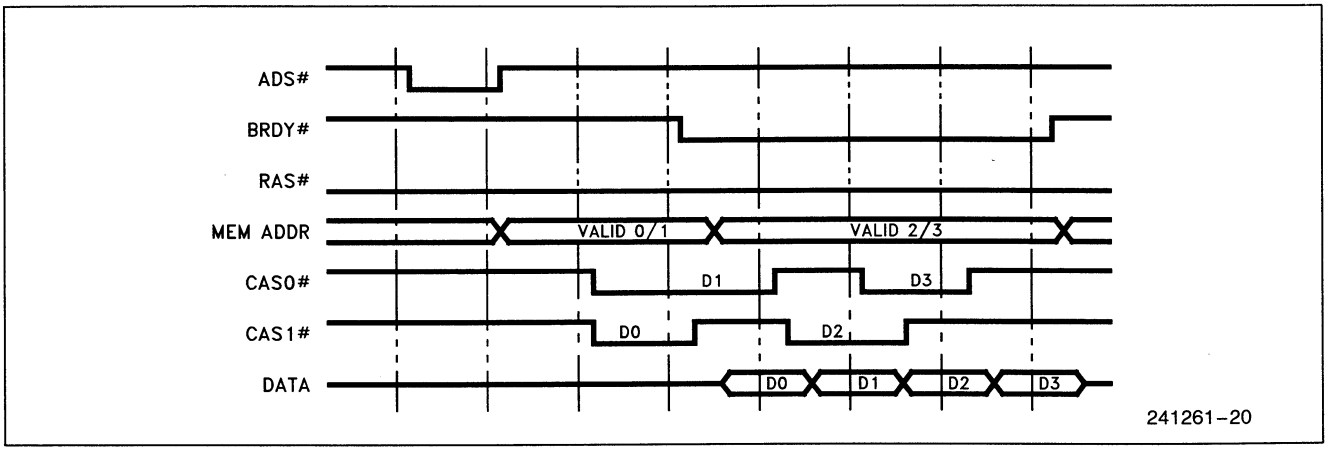


Figure 3.3. Burst Read Cycle from a Paged-Interleaved Memory System

Some implementations of a two-bank interleaved memory may be limited to a 1-2-1 burst cycle for the last three dwords. This is mainly limited by the amount of time it takes to invert the A3 address line between the second and third dwords.

3.3 Memory Read Performance Considerations

Seven memory systems with different read performance parameters are examined; write performance is kept constant during these simulations. The memory parameters are as follows:

Systems A through D represent the performance of some typical page mode memory controllers while the performance of systems E through G would require a paged-interleaved memory controller.

Table 3.2. Memory Systems used for the No-Cache System Test

	Read Page Hit	Read Page Miss	Write Page Hit	Write Page Miss
System A	4-3-3-3	8-3-3-3	3	6
System B	4-2-2-2	8-2-2-2	3	6
System C	4-2-2-2	7-2-2-2	3	6
System D	3-2-2-2	8-2-2-2	3	6
System E	3-1-2-1	7-1-2-1	3	6
System F	3-1-2-1	6-1-2-1	3	6
System G	3-1-1-1	6-1-1-1	3	6

The results for the Intel486 DX2 CPU with these memory systems is shown in Figure 3.4 through Figure 3.6 for the SPEC1, Pagemaker and Turbo C traces used previously. The graphs show the total execution time relative to the ideal zero-wait state memory system.

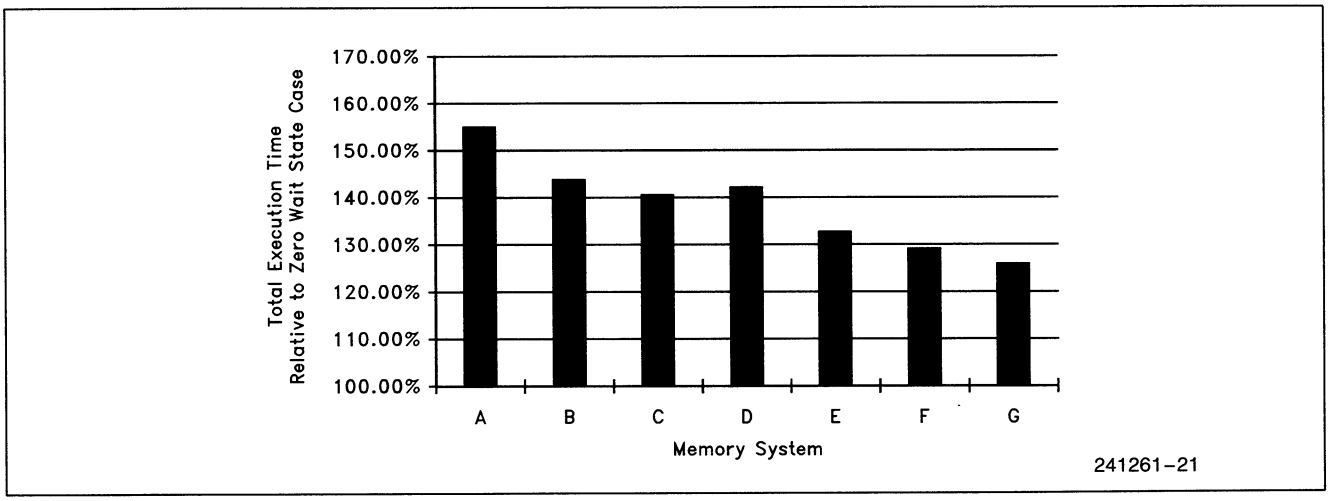


Figure 3.4. Total Intel486 DX2 CPU Execution Time versus Memory Read Performance - for SPEC1 (UNIX)

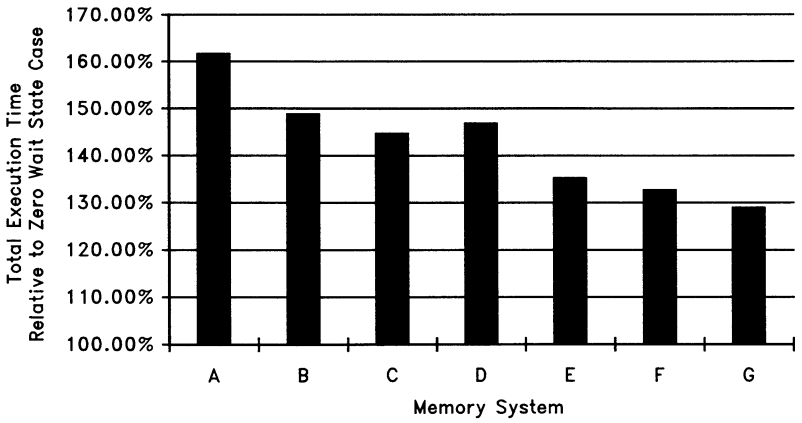


Figure 3.5. Total Intel486 DX2 CPU Execution Time versus Memory Read Performance - for Pagemaker (Windows)

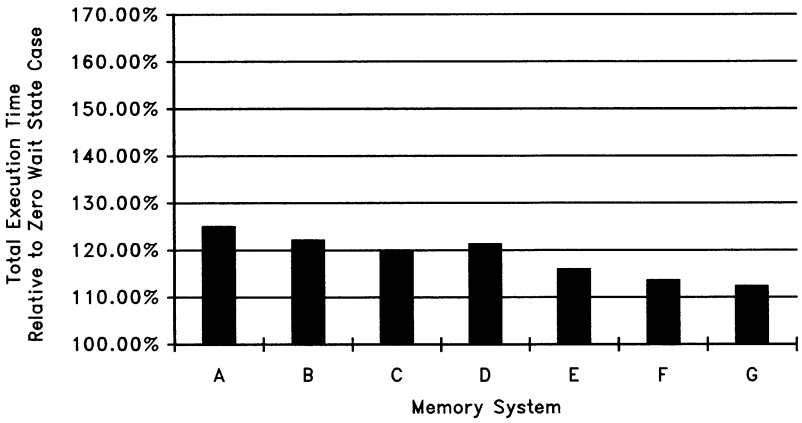


Figure 3.6. Total Intel486 DX2 CPU Execution Time versus Memory Read Performance - for Turbo C (DOS)

The interesting points to note here are:

- As expected, the DOS application suffers the least from slow memory performance.
- Burst performance is very important. Note the improvement from system A to B, system D to E and even from system F to G (where one clock was removed from the third burst).
- Since the read page hit ratio is lower than 50%, improving the read page miss lead-off cycle is more important than the read page hit lead-off cycle. Note the improvement from system B to C versus the improvement from system B to D.

3.4 Memory Write Performance Considerations

There are several methods of improving the write performance of the memory system. These methods are first described; the benefits of the different methods are discussed later.

The most common method for improving write performance is to employ page mode accesses to DRAM. As shown in Table 3.1, the page hit ratios for write cycles favor the use of page mode accesses. An example of a DRAM write cycle is shown in Fig. 3.7. On page hits, back-to-back three clock write cycles can be maintained. A page miss write would of course take an additional number of clocks to allow for the RAS# precharge time.

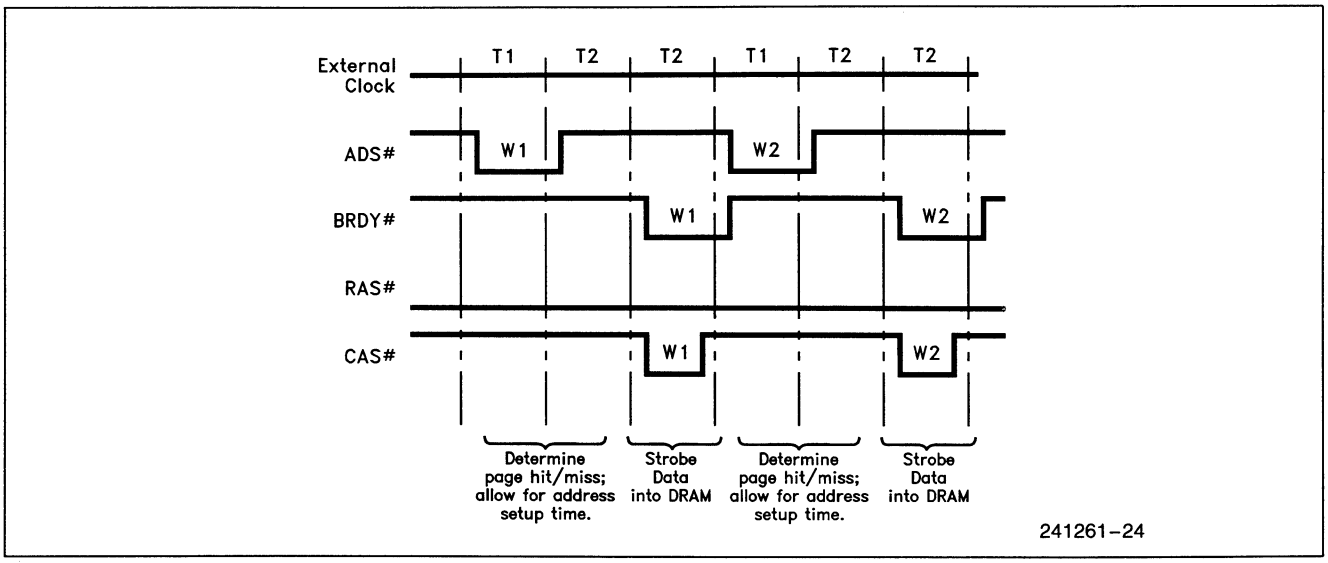


Figure 3.7. Page Mode DRAM Allow for Fast Back-to-back Writes

Memory write performance can be improved further by two related methods: write buffering and pipelining. If one external write buffer is added to the memory system shown in Fig. 3.7, the write cycles in Fig. 3.8 may be observed:

In the example shown, the one level of write buffering allows the first ready signal to be returned one clock earlier. The first write cycle finishes in two clocks (zero wait states); however, if the CPU puts out many back-to-back writes (as is typical), the memory system will still be limited to a throughput of three clock writes subsequent to the first write cycle. If the CPU write is not followed immediately by any bus traffic, the one write buffer does relieve the CPU quickly, especially if the write was a page miss.

More than one level of write buffering is sometimes employed. This would allow multiple writes to be accepted at zero wait states before wait states of the main memory system affect the CPU bus. To get the maximum benefit from multiple write buffering, CPU reads that occur when there are more than one writes pending in the external write buffers should be allowed to bypass the writes and be executed as soon as the existing memory write is complete. This is similar or course to the internal write buffers of the Intel486 CPU. If the read cycle's address corresponds to an address already in the write buffers, the read must wait until the corresponding write completes so that the read does not fetch stale data from memory. In other words, care must be taken to ensure data consistency when using external write buffers.

Write pipelining extends the use of buffering by overlapping the memory controller operations during the write cycle. An example is shown in Fig. 3.9 below. The data phase of the last write cycle (CAS# pulse) is overlapped in time with the address phase of the next memory write cycle (Page hit/miss decoding, etc.).

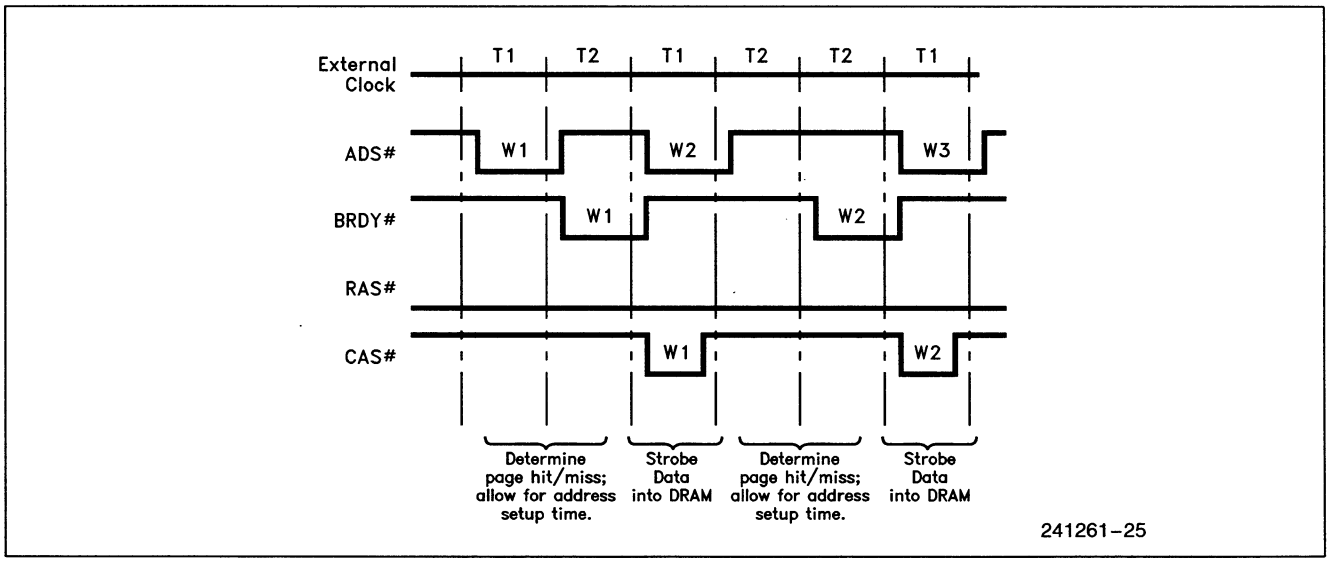


Figure 3.8. Adding One Write Buffer to the Memory System

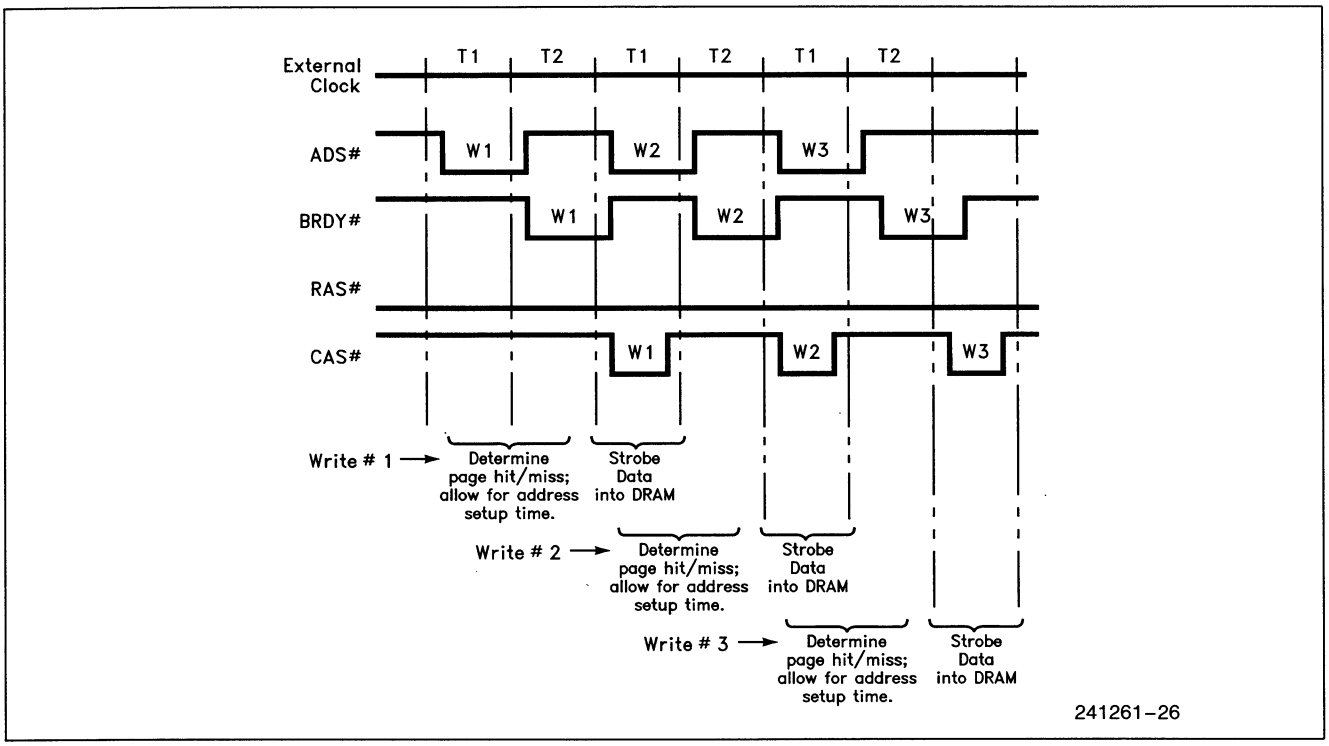


Figure 3.9. Pipelining the Writes to Memory

With pipelining, it is possible to achieve a throughput of many two-clock back-to-back page hit writes. (An example of write pipelining can be found in Intel Applications Note AP447) Note that pipelining may affect a subsequent read cycle; if the CPU read occurs immediately after the write, the beginning of the read will be delayed until the DRAM write cycle has completed. This is especially true for page miss writes where the write may take several clocks to complete. Note also that pipelined memory write systems can be combined with write buffering; this helps for the case where many back-to-back page miss writes occur.

Note that both write buffering and/or pipelining require a data path device between the CPU and main memory (see Fig. 3.10). This is needed to capture the data from the CPU before RDY# or BRDY# is returned, after which point the data will become invalid.

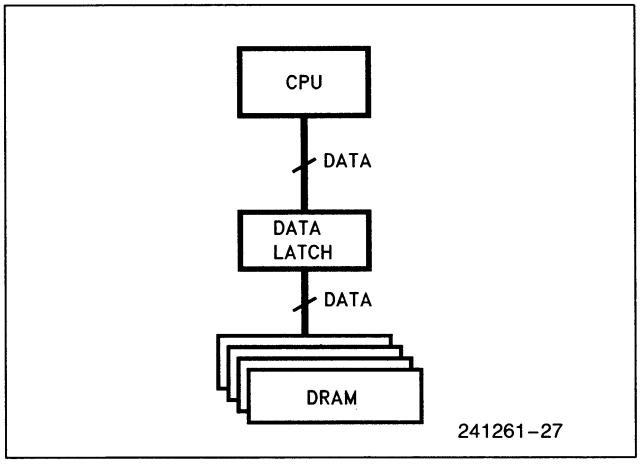


Figure 3.10. A Data Latch is Required for Write Buffering or Pipelining

To understand the performance benefits of the various methods described, systems B and F from the earlier simulations for read performance are repeated with different write performance parameters (refer to Table 3.3). Systems B and F were chosen as typical representations of paged and paged-interleaved memory controllers respectively.

Table 3.3. Memory Systems with Different Write Performances

	Read Pg Hit	Read Pg Miss	Write Pg Hit	Write Pg Miss	Write Method
System B1	4-2-2-2	8-2-2-2	3	6	Normal
System B2	4-2-2-2	8-2-2-2	3	6	One buffer
System B3	4-2-2-2	8-2-2-2	2	6	Pipelined
System B4	4-2-2-2	8-2-2-2	2	5	Pipelined
System B5	4-2-2-2	8-2-2-2	2	5	Pipelined with two buffers
System B6	4-2-2-2	8-2-2-2	2	5	Pipelined with four buffers
System F1	3-1-2-1	6-1-2-1	3	6	Normal
System F2	3-1-2-1	6-1-2-1	3	6	One buffer
System F3	3-1-2-1	6-1-2-1	2	6	Pipelined
System F4	3-1-2-1	6-1-2-1	2	5	Pipelined
System F5	3-1-2-1	6-1-2-1	2	5	Pipelined with two buffers
System F6	3-1-2-1	6-1-2-1	2	5	Pipelined with four buffers

The memory systems above were simulated again for the Intel486 DX2 CPU with the three applications. The results are shown in Fig. 3.11 through Fig. 3.13 below:

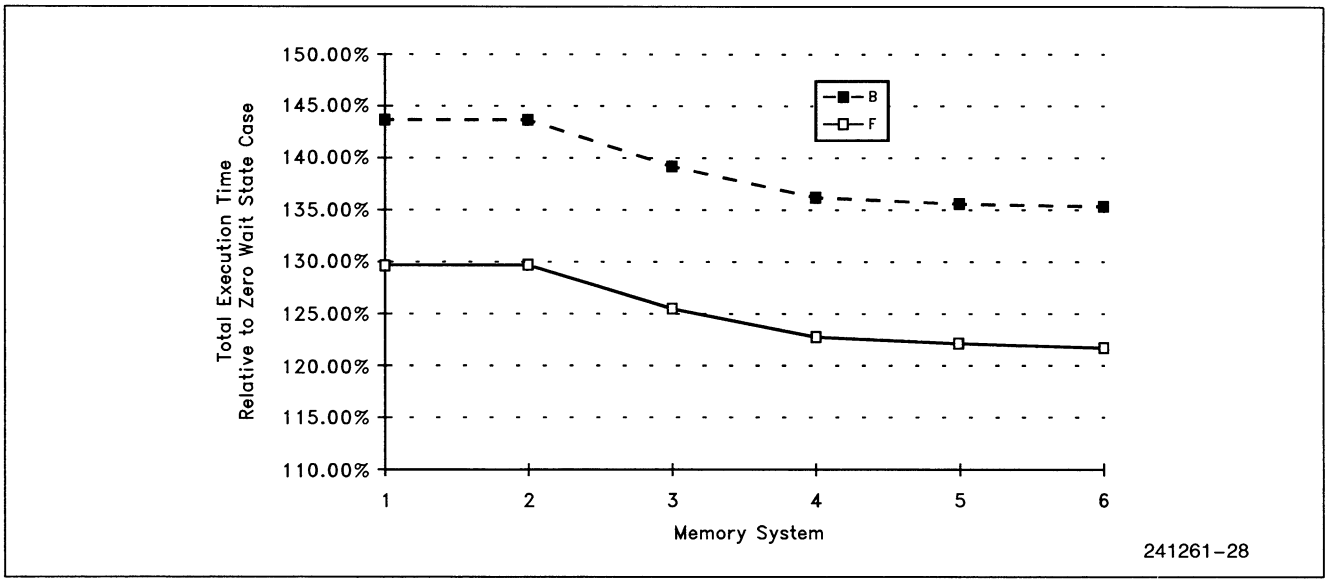


Figure 3.11. Total Execution Time versus Write Performance- for SPEC1 (UNIX)

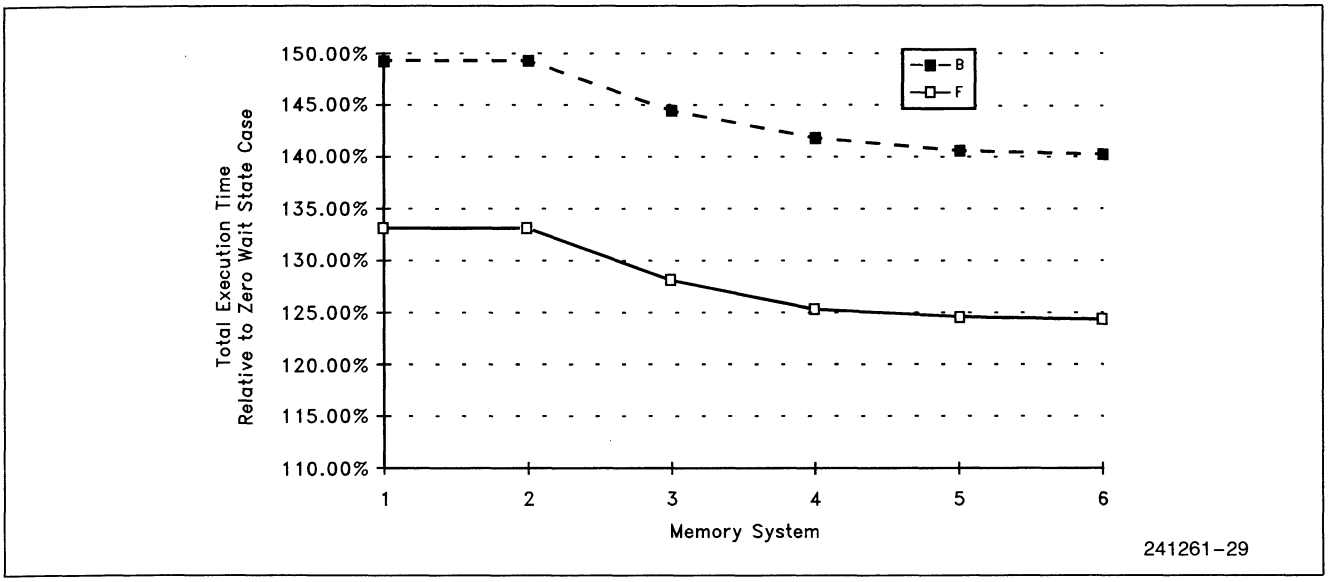


Figure 3.12. Total Execution Time versus Write Performance - for Pagemaker (Windows)

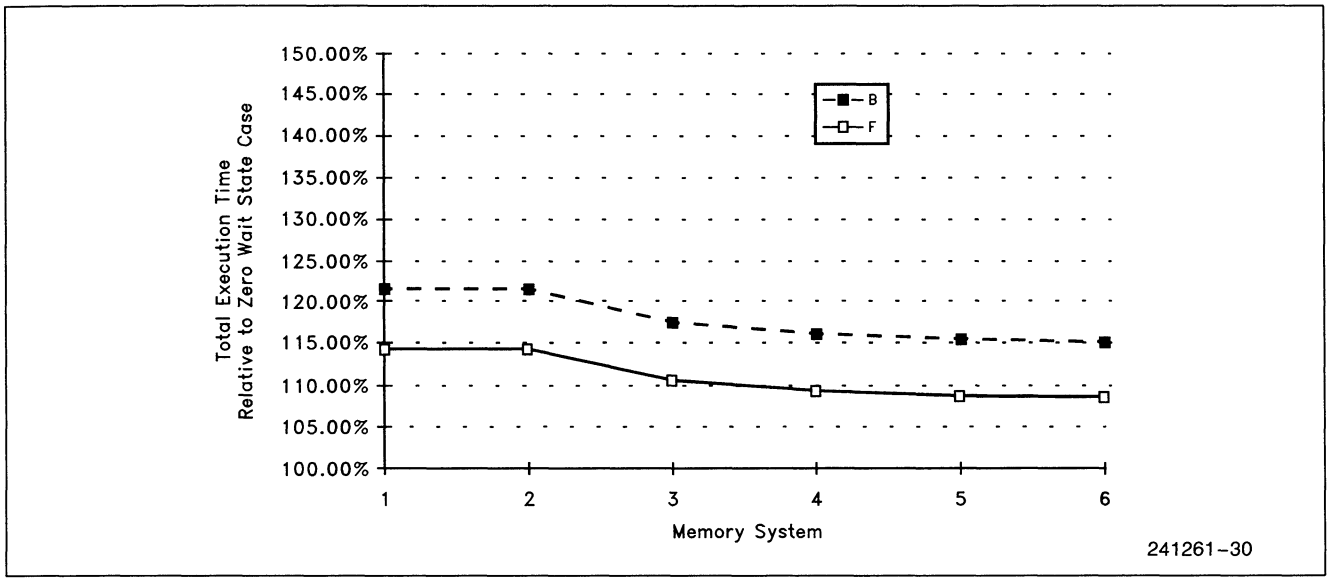


Figure 3.13. Total Execution Time versus Write Performance - for Turbo C (DOS)

From the results shown, the following significantly improved CPU performance:

- Reducing the number of clocks for page hit writes (system B2 to B3 and F2 to F3)
- Reducing the number of clocks for page miss writes (system B3 to B4 and F3 to F4)

The following caused marginal improvement in the execution time:

- Adding one level of buffering (from memory systems B1 to B2 and F1 to F2)
- Adding more than two write buffers (from B4 to B5 to B6 and F4 to F5 to F6) resulting in only a 1-2% improvement.

These results may be somewhat surprising considering the earlier graph showing performance degradation as the number of write wait states increases (Fig. 3.7). One would expect that adding write buffers would compensate for the slower memory write system more than they do. In order to understand the results, consider the statistics in Table 3.4 for processor execution stalls as a result of write activity as described in Section 2.5.3. The statistics are shown for the SPEC1 trace.

Note that the Stalls Because of Reads On Busy Writes dominates the increase in execution time for memory system F1 compared to the zero wait state case. Adding one write buffer (from system F1 to F2) - in an attempt to improve performance - decreases the percentage of stalls on a full write buffer from 5.3% to 4.5%. However, while the number of Stalls Because of Reads on Busy Writes did decrease, the wait states were simply transferred to stalls while waiting for the first ready of a read and no net imp rovement is observed. One example of this situation is illustrated in Fig. 3.14.

Table 3.4. Stall Statistics for the Write Buffers for the SPEC1 (UNIX) Trace

	Percentage of Total Execution Time Stalled:			
	On Write Buffers Full	**Because of reads on Busy Writes**	**Because a Read Cannot Overtake a Write**	**Waiting for First Ready**
Zero Wait State Case	1.0%	2.4%	0.3%	8.8%
Memory System F1	5.3%	8.0%	0.5%	17.1%
System F1 plus one write buffer	4.5%	4.9%	0.4%	20.9%

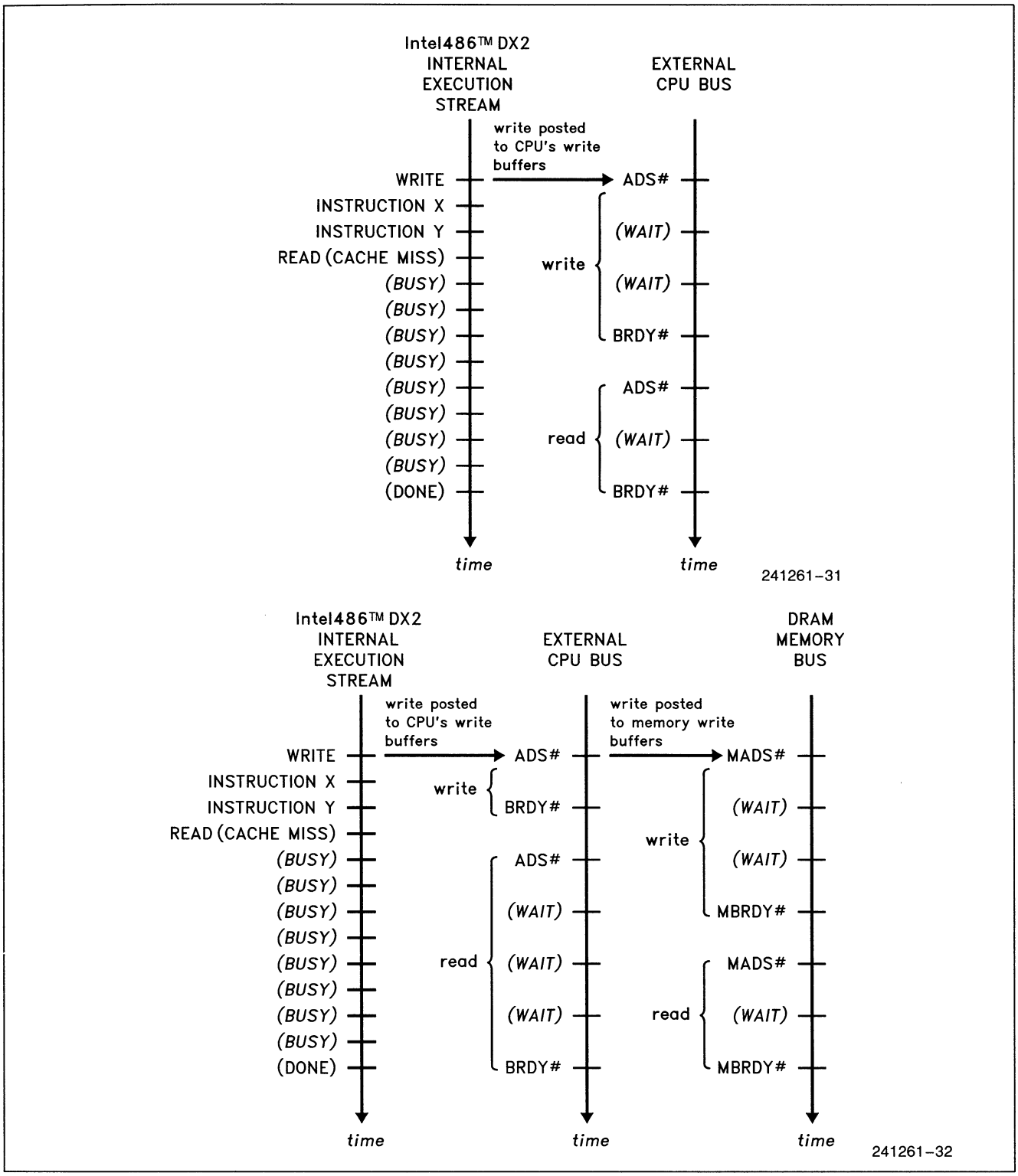


Figure 3.14. Adding Write Buffers Does Not Improve Stalls Because of Reads on Busy Writes

In the example shown, without external memory write buffers, the cache miss read shown stalls for four clock cycles while waiting for the write cycle to complete. With memory write buffers, the CPU need not wait to start the read cycle since the write completed in zero wait states. However, since main memory is still occupied with the original write cycle, the read is still delayed externally while the write completes. The net effect is that the read-stalls because of write traffic does not decrease; th e write traffic has simply been transferred from the CPU bus to the memory bus where it has to contend with the next read cycle.

Note that there will be instances where the addition of external write buffers to a cacheless memory system does benefit a sequence of bus cycles. This would be the case for applications with very low external read traffic and large amounts of write traffic. In this case, the write buffers do benefit the heavy write traffic while the reads on busy writes will be a lower percentage of total stalls.

3.5 Viability of Intel486 DX2 System without an External Cache

As shown in this section, the CPU performance of a cacheless, main-memory-only Intel486 DX2 CPU based system will range from good to fair depending on the application. The correct cost-performance point will dictate the viability of such a product. For the Windows and UNIX applications tested, with a good memory design, the Intel486 DX2 CPU will get to about 120% of the execution time of the ideal zero wait state case with the examples shown. The reciprocal of total execution time is CPU performance; wh ich works out to 83% of maximum in this case. Of course, other system design factors will come into play, such as refresh requirements, other bus master memory requirements, etc.

More exotic memory architectures may improve the performance of the cacheless Intel486 DX2 CPU system design over what has been discussed here. However, the next section will address the more straightforward method of increasing CPU performance further: adding an external cache.

4.0 CACHE DESIGN OPTIMIZATION

An external cache will supplement the on-chip 8K cache of the Intel486 DX2 CPU. The requirement for an external cache is more important for the Intel486 DX2 CPU than it was for the Intel486 DX CPU for all the reasons discussed in the previous sections.

Many cache architectures have been implemented with the Intel486 DX CPU. Caches differ depending on their size, associativity, serial vs. parallel implementations, write-through vs. write-back policies, etc. This section will focus on optimizing the performance of a uniprocessing system, i.e. the CPU is the major consumer of main memory bandwidth. The architectures discussed are shown in Figure 4.1.

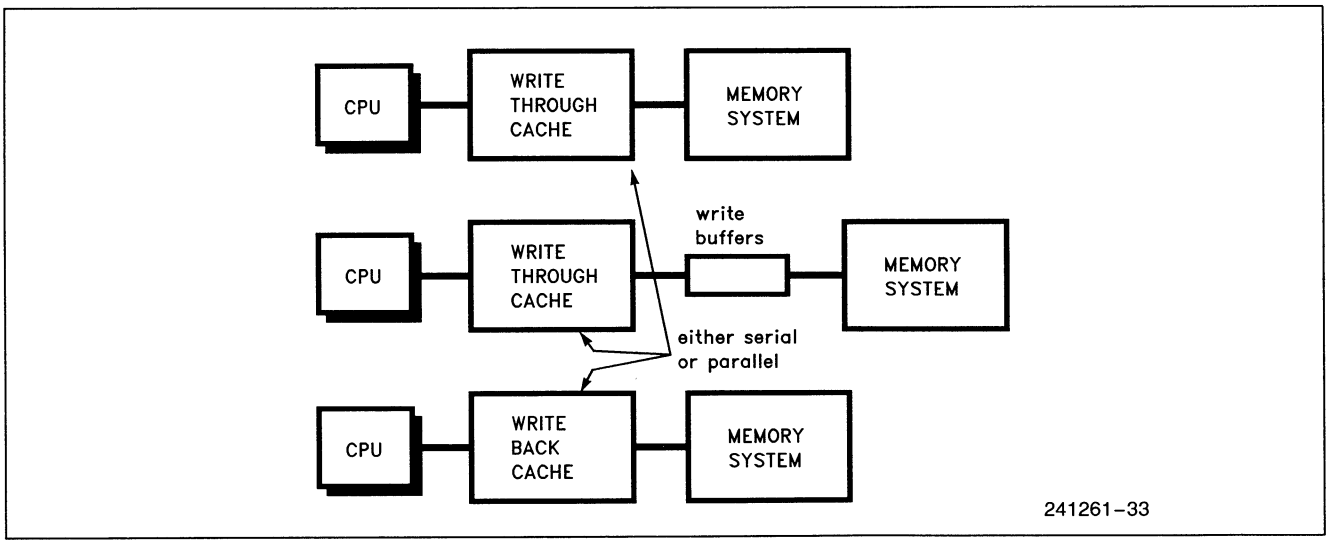


Figure 4.1. Different Cache Architectures Discussed

4.1 Overall Effect of an External Cache on CPU Performance

The same memory systems tested in the previous section are tested again with a 128K 2-way associative write-through parallel cache. This will yield the improvement achieved by the decrease in the effective number of read and burst wait states. The results are shown in Figures 4.2 through 4.4 for the three applications tested earlier.

The addition of an external write-through cache reduces the performance degradation caused by main-memory wait states for the lead-off cycle of a read and for wait states during the remainder of a burst. The impact of these wait states was discussed in Section 2.5.3.

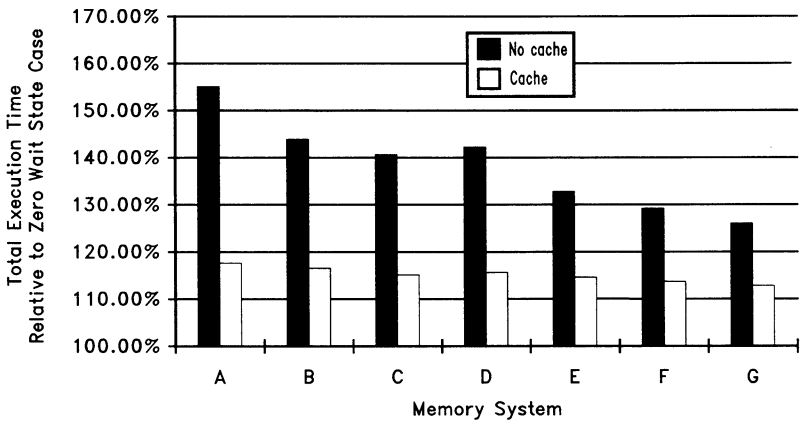


Figure 4.2. Adding an External Cache Decreases Execution Time - for SPEC1 (UNIX)

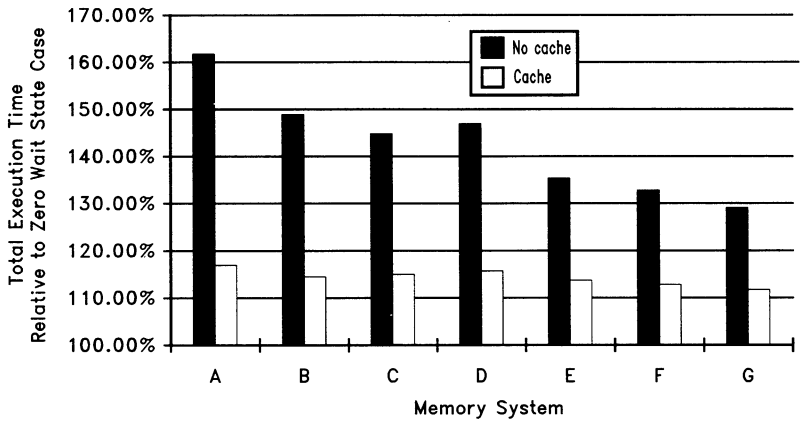


Figure 4.3. Adding an External Cache Decreases Execution Time - for Pagemaker (Windows)

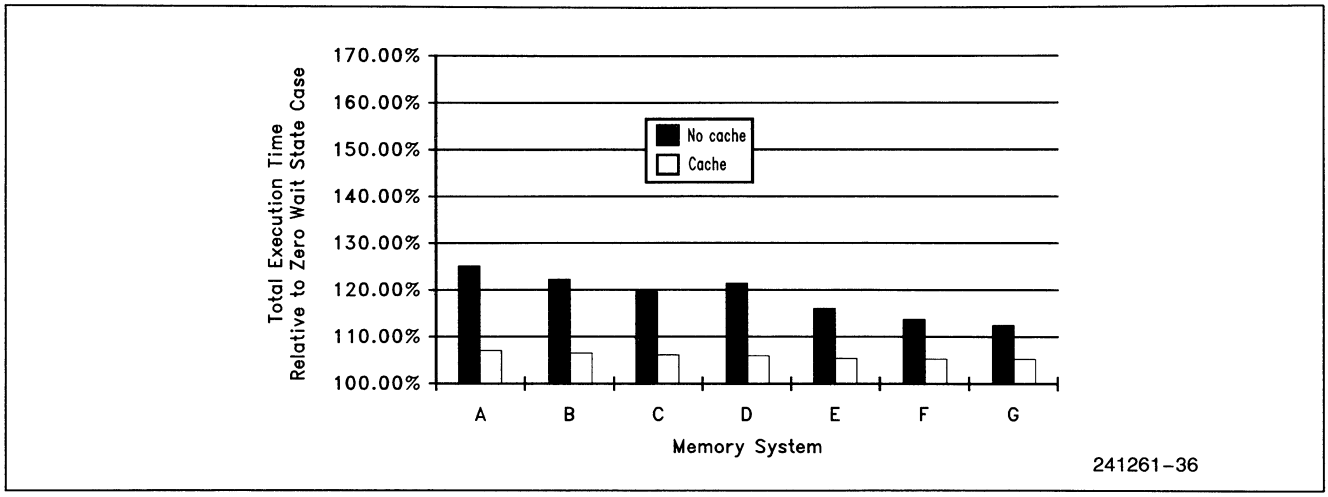


Figure 4.4. Adding an External Cache Decreases Execution Time - for Turbo C (DOS)

For the UNIX and Windows applications, the addition of the external cache improved the execution time by 15%-35% depending on the memory design. The cache used in this case - a 128K two-way set associative cache - does an excellent job of buffering the CPU performance from the memory system performance. However, note that even with the external cache, the execution time is still 12%-18% above the zero wait state case for these two applications. This is due to the write performance of the memory system s ince the cache policy in this example is write-through. Further improvement on the write performance is investigated later in this section.

For the DOS application, the addition of the cache brings the performance of the Intel486 DX2 within 5% of the ideal zero wait state case. This is of course due to the lower miss rate of the CPU's internal cache and the application's low bus utilization.

4.2 Effect of Cache Size and Associativity

A 128K two-way-associative, write-through, parallel, external cache was used in the previous section. As the size and associativity of the cache are varied, the CPU performance varies. This is shown in Fig 4.5 for the memory systems B and F as used earlier (see Table 4.1). Both one-way (direct mapped) and two-way set associative caches are tested with the SPEC1 application trace.

Table 4.1. Memory Systems for the Write-Through Cache Test

	Read Page Hit	Read Page Miss	Write Page Hit	Write Page Miss
System B	4-2-2-2	8-2-2-2	3	6
System F	3-1-2-1	6-1-2-1	3	6

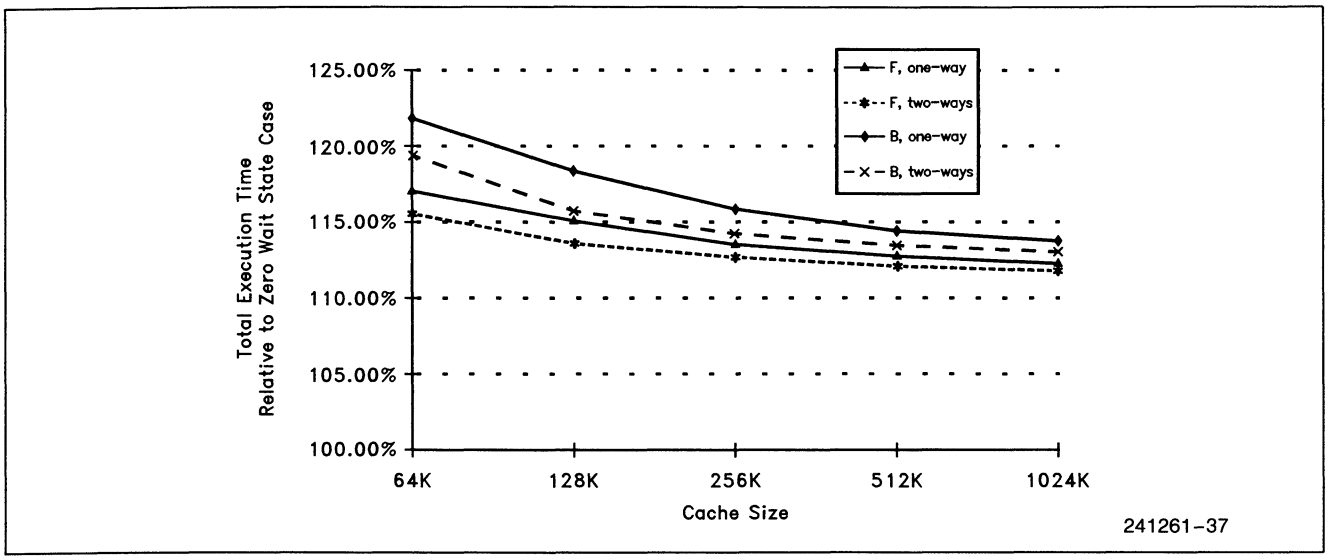


Figure 4.5. Total Execution Time for the Intel486 DX2 CPU as a Function of Cache Size and Associativity - for SPEC1

Fig 4.6 illustrates the external cache hit rates for CPU read cycles. The hit rates are directly related to the total execution time; higher hit rates result in shorter execution times.

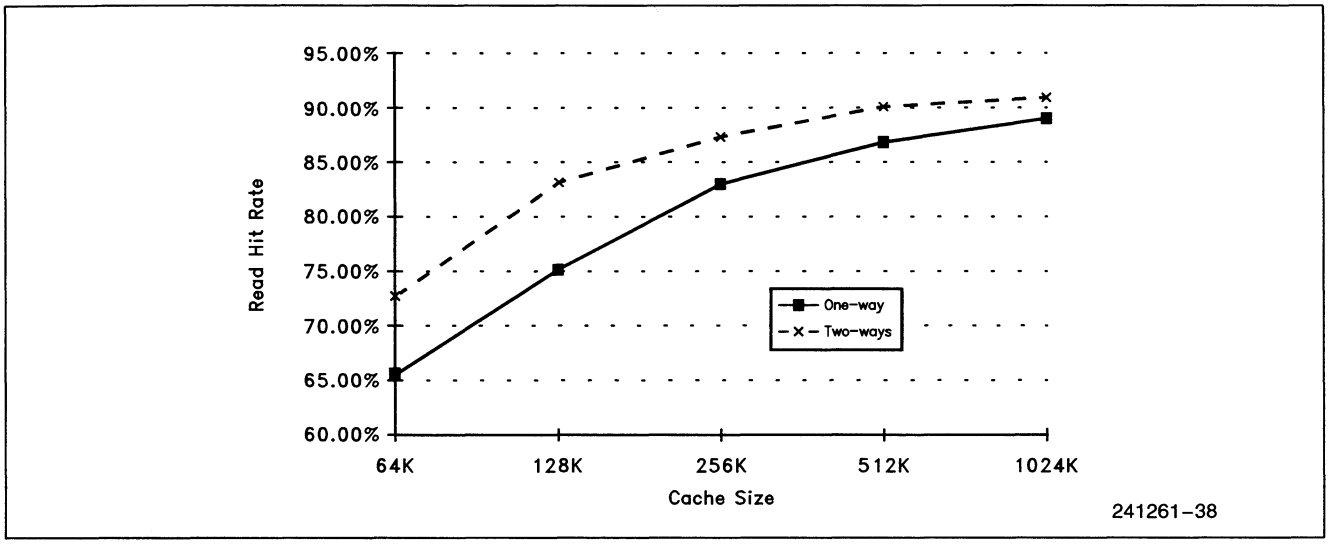


Figure 4.6. L2 Read Hit Rate as a Function of Cache Size and Associativity (UNIX)

4.3 Improving the Performance of a Write-Through Cache

With a write-through cache, good memory write performance is necessary to achieve the best possible performance with the Intel486 DX2 microprocessor. All of the methods for improving the write performance for a cacheless system, discussed in section 3.4, also apply for the write-through cache-based system.

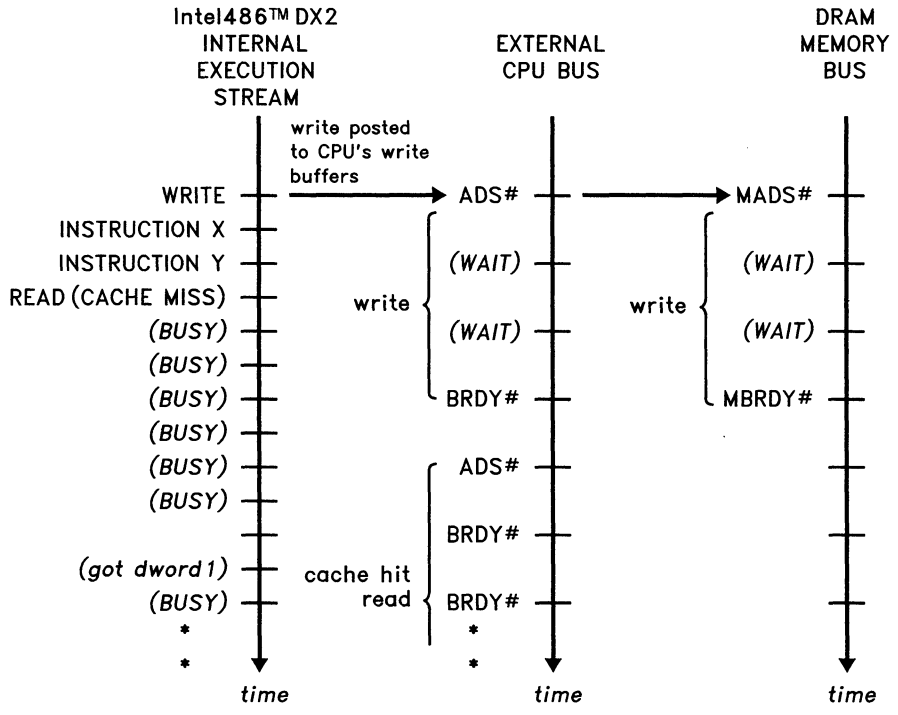
4.3.1 MEMORY WRITE PIPELINING

The previous results for a write-through cache assumed a non-pipelined memory system with a page-hit write performance of three clocks and a page-miss performance of six. The most effective method of increasing the memory write performance further is the use of memory write pipelining. The write performance can be improved so that continuous back-to-back page-hit write cycles can complete in zero wait-states. Pipelining can also reduce the number clocks required for a page-miss write cycle. As the write performance improves using this technique, the write-through cache system can come close to that of the ideal zero wait state system. These results are shown in Section 4.3.3 to follow.

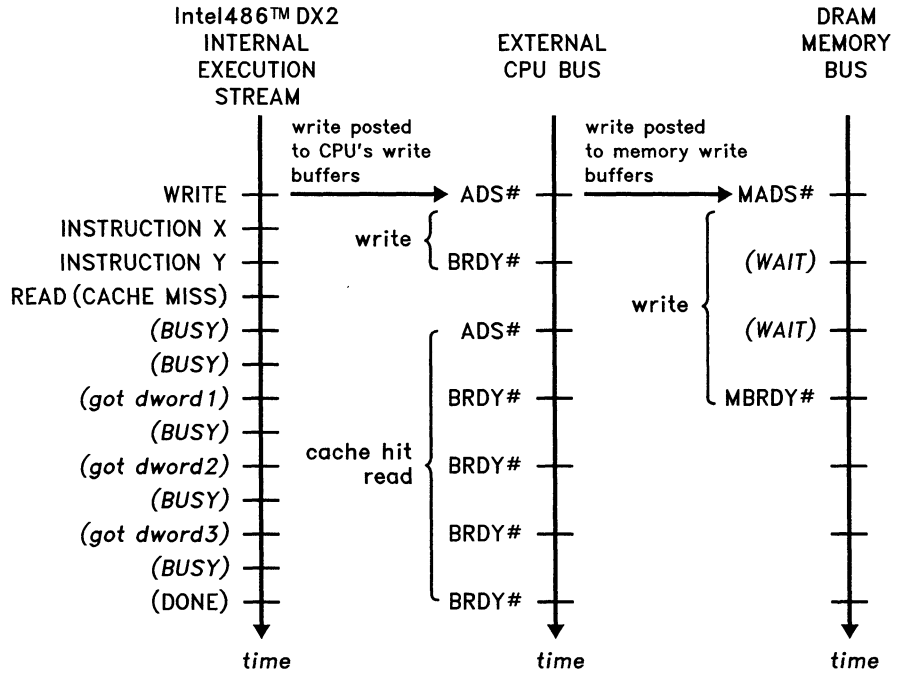
4.3.2 EXTERNAL WRITE BUFFERS

Adding one or more write buffers to a external write-through cache-based system improves performance by a larger amount compared to the cacheless case. Figure 4.7 illustrates why.

The addition of external write buffers allows the memory write cycle to be "hidden" from the CPU bus if the next CPU cycle happens to be a external cache hit read. And since the external cache read hit ratio is high, most of the delays which were present in a cacheless system under these circumstances are removed. In essence, the on-chip cache/write-buffers have been duplicated externally to provide a multiple level architecture (see Fig. 4.8).



Without Memory Write Buffers



With Memory Write Buffers

Figure 4.7. Adding External Write Buffers to an External Cache Reduces Execution Time

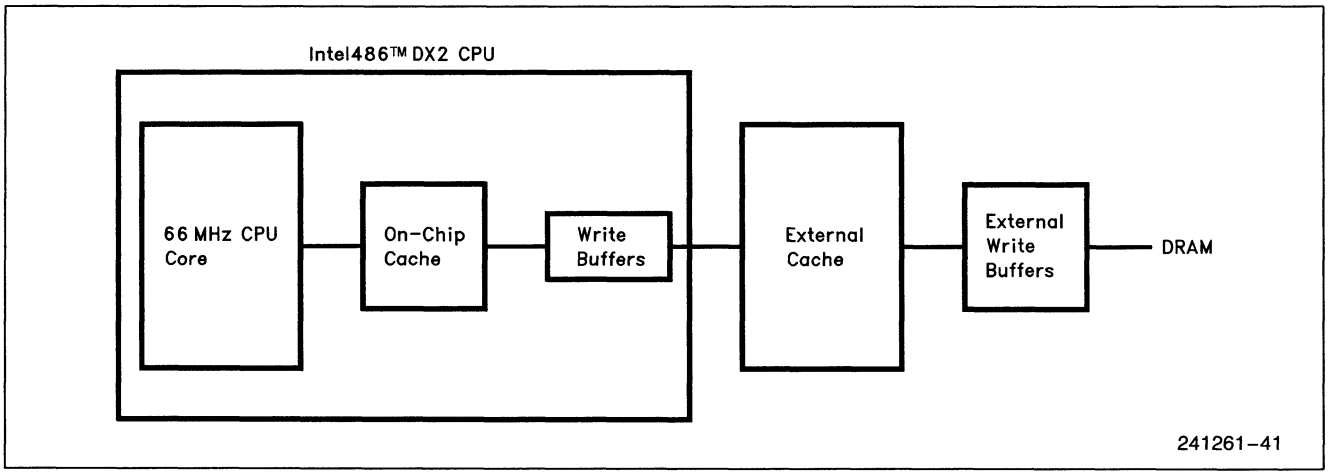


Figure 4.8. A Hierarchy of Caches and Write Buffers

4.3.3 PERFORMANCE WITH AN EXTERNAL WRITE-THROUGH CACHE

To quantify the benefits of improving the write performance, the systems in Table 4.2 were tested.

Table 4.2. Memory Systems Used for Write-Through Cache Test

	Read Pg Hit	Read Pg Miss	Write Pg Hit	Write Pg Miss	Write Method
System B1	4-2-2-2	8-2-2-2	3	6	Normal
System B2	4-2-2-2	8-2-2-2	3	6	One buffer
System B3	4-2-2-2	8-2-2-2	2	6	Pipelined
System B4	4-2-2-2	8-2-2-2	2	5	Pipelined
System F1	3-1-2-1	6-1-2-1	3	6	Normal
System F2	3-1-2-1	6-1-2-1	3	6	One buffer
System F3	3-1-2-1	6-1-2-1	2	6	Pipelined
System F4	3-1-2-1	6-1-2-1	2	5	Pipelined

Fig. 4.9 shows the results of the memory systems tested with a 128K, two-way associative, write-through, parallel cache and the Intel486 DX2 CPU using the SPEC1 application trace.

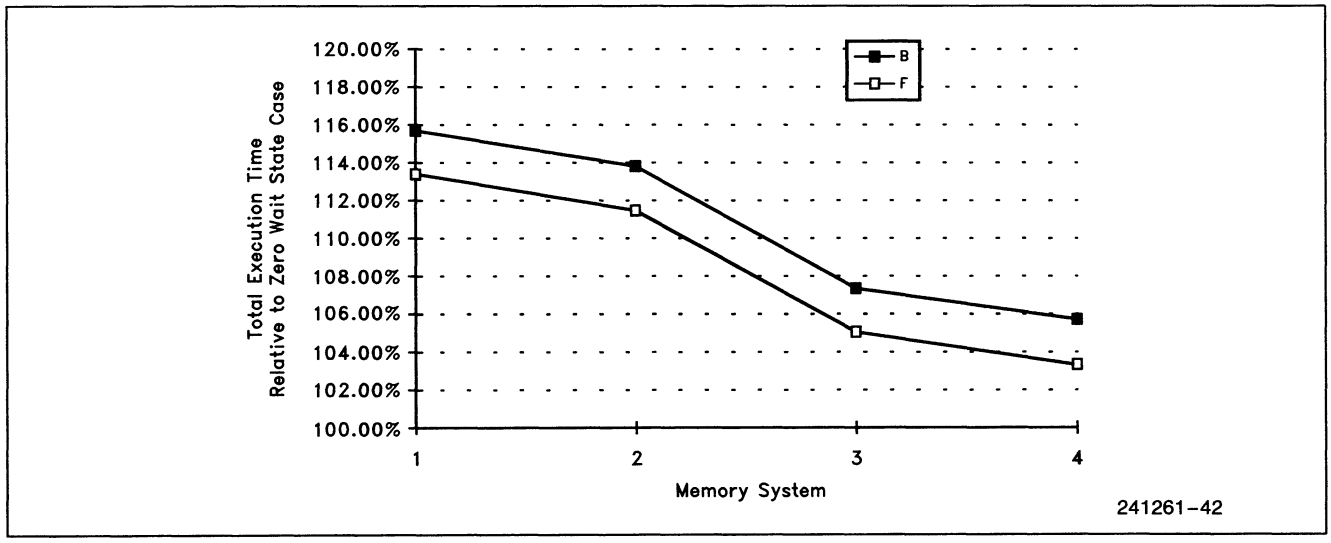


Figure 4.9. Improving the Write Performance Benefits a Write Through Cache - for SPEC1

As the write performance increases, the CPU performance approaches that of the zero wait state case. The improvement from systems B1 to B2 and from F1 to F2 illustrate the benefit of write buffering with an external cache. The improvement from systems B2 to B3 and from F2 to F3 reflect the benefit of memory write pipelining. Finally, the improvement from systems B3 to B4 and from F3 to F4 show how reducing the page-miss write performance also increases performance.

4.4 Write-Back Caches

If correctly implemented, a write-back external cache can provide good performance for a uniprocessing Intel486 DX2 CPU based system. Serial write-back caches have typically been used to reduce bus utilization for multiprocessing systems. The design complexity of a write-back cache controller is typically an order of magnitude higher than for a write-through cache controller. However, correct implementation is absolutely necessary if significant performance gains are to be realized with the Intel486 DX2 CPU.

A write-back cache is different from a write-through cache in that it allows cache write hits to modify the cache line without updating main memory. The cache has tags that include a bit called the modified (dirty) bit. This bit is set if the cache location has been written with new information and therefore contains information that is more recent than the corresponding information in main memory. If a subsequent read miss occurs and the line being fetched needs to fill the cache location that is currently being occupied by the modified line, the cache controller must then write the modified cache line back to main memory; hence coherency is maintained.

If a CPU write is not a cache hit, the cache controller has the option of allowing the write to propagate through to memory or to fetch the cache line from memory to be merged with the new write data. The cache line fill in the second option is called a write-allocation. In the following discussions, it is assumed that no write-allocations are being performed.

4.4.1 MAIN MEMORY CONTROLLER CONSIDERATIONS

The addition of an external write-back cache changes the characteristics of the main memory bus traffic. Since the cache effectively filters all CPU requests, the cycles that do propagate to main memory tend to be more distributed in their locations. This decrease in temporal and spatial locality will reduce the DRAM page hit rate as shown in Table 4.3 for a 128K, two-way associative, write-back cache with the SPEC1 application trace. Compare these results to the prior results in Table 2.1 for a cacheless system.

Table 4.3. Page Hit Ratios for a Write-Back Cache - for SPEC1

MEMORY CYCLES (100%)		SPEC1	PGMK	TURBOC
Reads:	Page Hits	17.1%	25.6%	24.7%
	Page Misses	13.8%	13.9%	12.9%
Writes:	Page Hits	58.9%	55.8%	40.8%
	Page Misses	10.2%	4.7%	21.6%

Therefore, it is less beneficial with a write-back cache to implement a page-mode main memory controller.

Of course, page mode DRAM accesses within the burst cycle are still important to retrieve the four words of a cache line quickly. This is also true for the write-back cycle where four dwords of the cache line must be written to memory. Memory controllers should be designed to support a burst write cycle instead of having to write each dword separately.

4.4.2 WRITE-BACK CYCLE

The write-back cycle is the sequence where a cache line fill from main memory has to displace a modified line that was already in the cache. The method in which the modified line is written back to main memory has an impact on overall CPU performance. Before analyzing the write-back cycle, consider first the architectures shown in Fig. 4.10.

In the simplest implementation, a write-back cache will share the data bus with the CPU and main memory as shown in configuration X. If this is the case, then during a write-back cycle, the modified line must be written back to main memory before the cache linefill can commence. This has a detrimental effect on performance since the CPU must wait while the write-back occurs. This sequence is shown in Figure 4.11.

With a data path device between the CPU-Cache bus and main memory as shown in configuration Y, the cache controller is able to defer the write-back of the modified data till after the linefill has completed. The CPU can continue execution after the linefill as long as subsequent cycles are all cache hits.

In configuration Z, a wider cache bus exists between the SRAM and the data path devices. This allows the modified data to be transferred more quickly from the SRAM to the data path device, thereby allowing the cache linefill to commence even sooner.

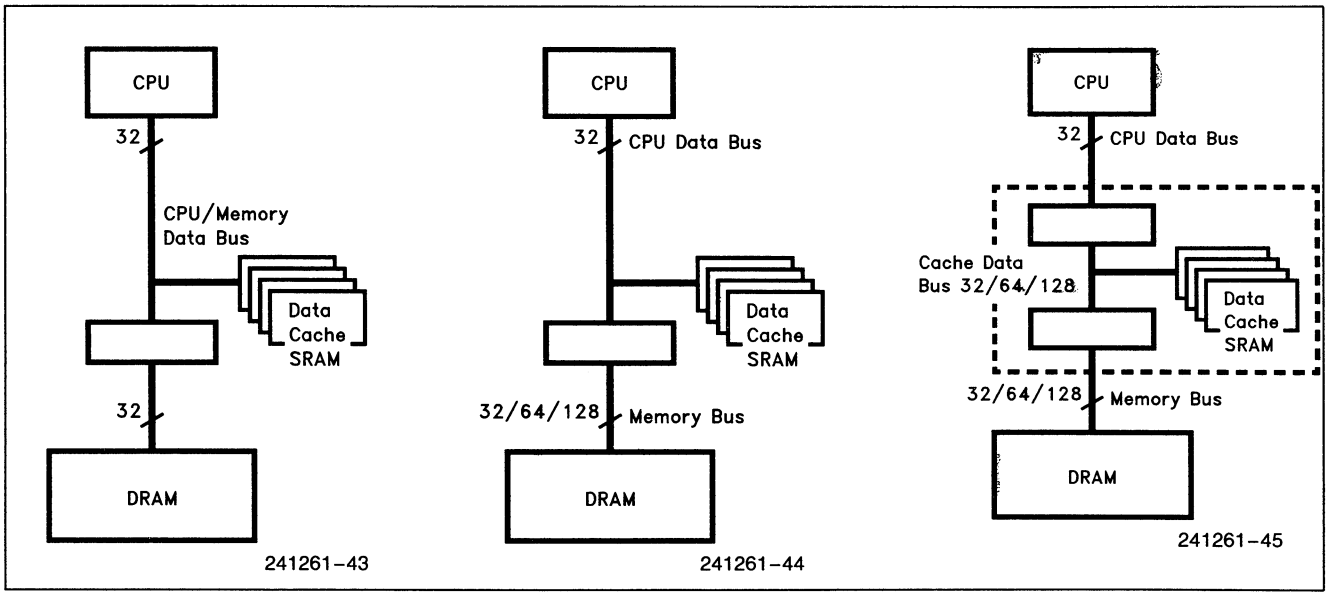


Figure 4.10. Different Architectures will Effect CPU Performance with a Write-Back Cache

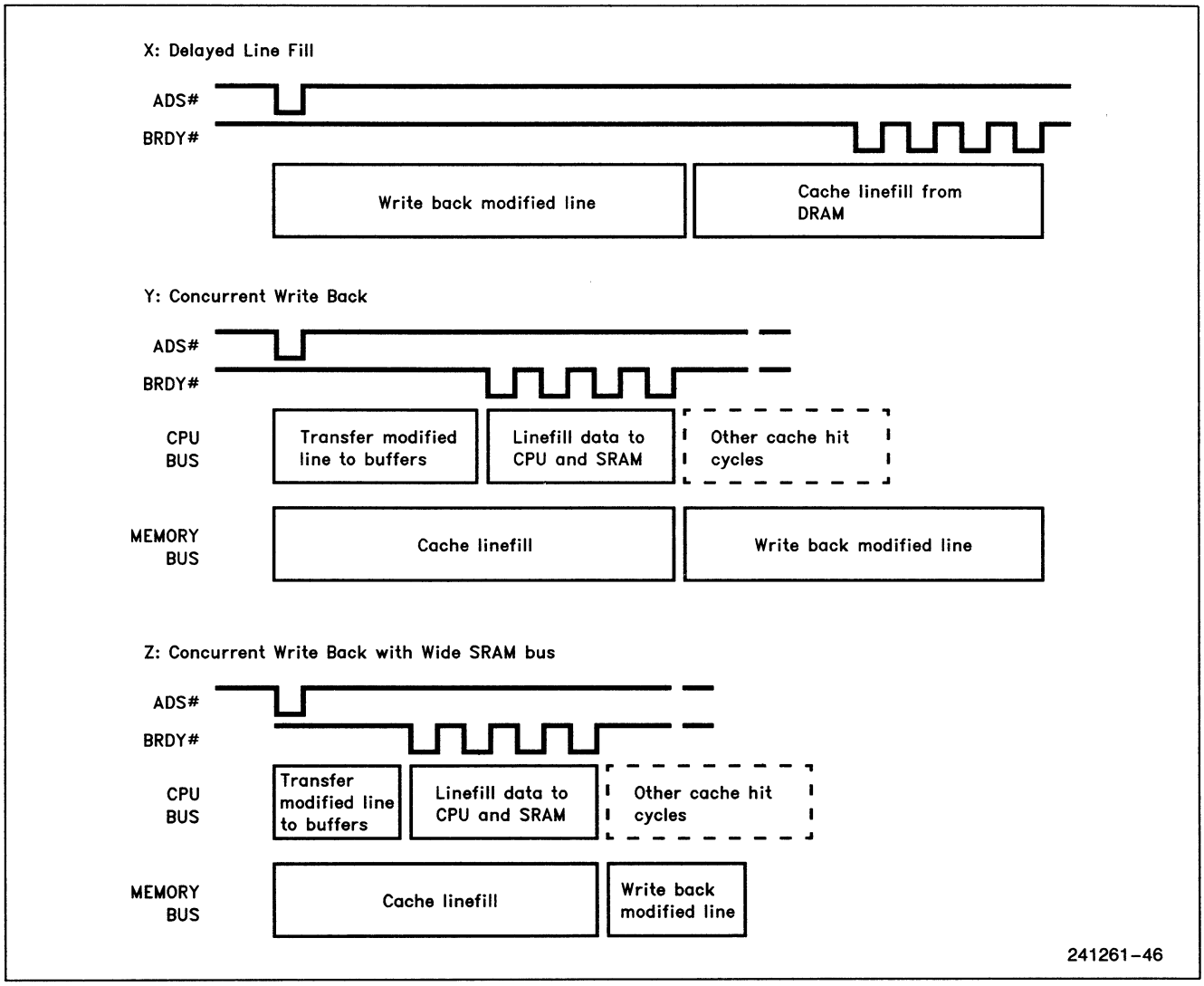


Figure 4.11. Different Implementations of the Write-Back Cycle

The following systems are used to demonstrate Intel486 DX2 microprocessor performance with different cache sizes and associativities.

The results are shown in Fig. 4.12 for the Intel486 DX2 CPU running the SPEC1 trace.

Table 4.4. Memory Systems used for Write-Back Cache Test

	Reads	Writes	Write-Back Method (described above)
System A	5-1-1-1	4-1-1-1 (burst)	Concurrent Write Back
System B	6-3-3-3	4-4-4-4 (non-burst)	Concurrent Write Back
System C	6-3-3-3	4-4-4-4 (non-burst)	Delayed Line Fill

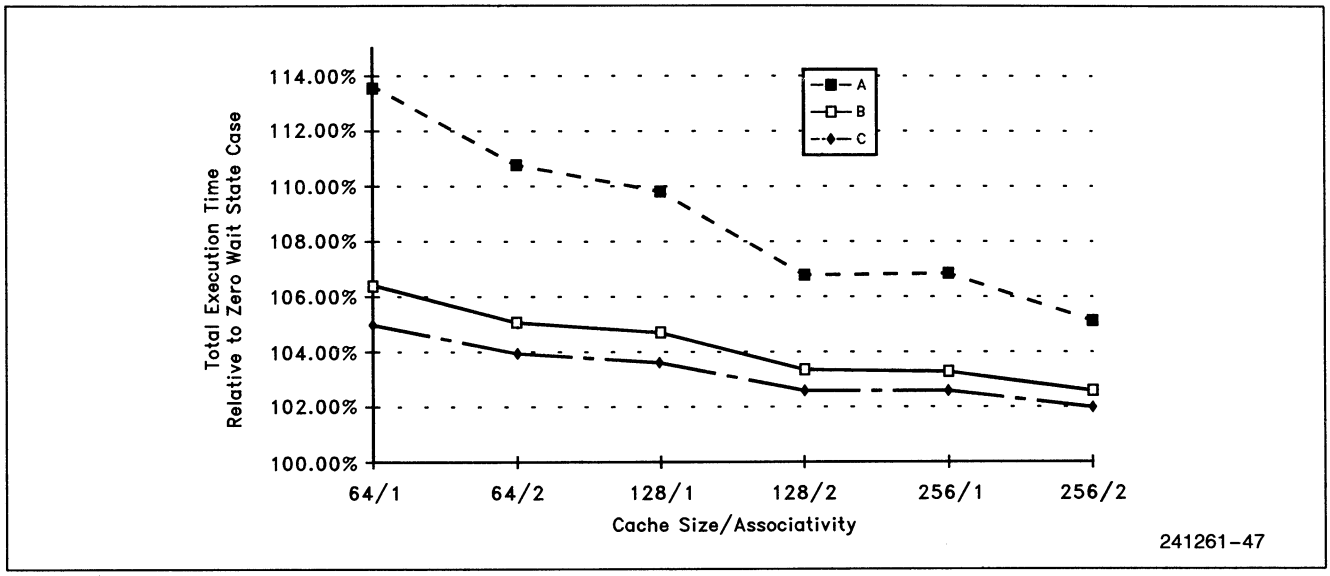


Figure 4.12. Intel486™ DX2 CPU Total Execution Time with Different Cache Size, Associativity, Memory Speed and Write-Back Method - for SPEC1

The addition of a write-back cache does an excellent job of decoupling the CPU performance from the main memory performance as shown with memory systems A and B. However, note that memory system B (with the delayed line fill) performs poorly - even worse than a good write-through cache - unless a significant amount of cache memory is added to reduce the miss rate.

5.0 CONCLUSION

This document has shown that good memory performance is especially important for the Intel486 DX2 microprocessor. Business workstation designs will require excellent CPU performance and will consequently have to incorporate well-designed, high-performance cache and memory systems.

In optimizing memory performance, an external cache is essential for hiding slow main memory access times. Write-through external caches offer good performance if coupled with good memory write performance. Write-back external caches can also offer excellent performance if designed correctly. Parallel write-back caches that cannot defer the write-back cycle till after a cache line fill will perform worse than a good write-through cache design.

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